Technical Manual

Hardware
Z-100 Series Computers

593-0038-04
CONSISTS OF

MANUAL
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TM-100

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About These Manuals

This technical manual set for the H/Z-100 Series of Desktop Computers (Low-Profile and All-in-One) is divided into a number of volumes for easy handling and quick reference.

- Hardware Volumes 1 and 2 — These two volumes contain disassembly information, module definitions, user options, theory of operation and programming information (of the hardware), parts lists, and schematics for your computer.

- Hardware Appendices — This volume contains reprints from various manufacturers and includes the S-100 bus specifications, IC data sheets and the iAPX 88 Book. Place this last item in this binder as it includes the 8088 architecture and instruction set.

- ROM Source listings — These volumes are printouts of the source code used in the various boot (monitor) ROM's that can be part of your system.

We have made every effort to give you up-to-date information in these volumes and it was considered to be correct at the time it was written. However, Zenith Data Systems Corporation may alter the products described herein from time to time and these changes may or may not be reflected in this publication. Zenith Data Systems Corporation reserves the right to make these changes without incurring any obligation to incorporated new features in products previously sold.

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Chapter 1 GENERAL INFORMATION

Introduction

The Z-100 Series Desktop Computers (Low-Profile and All-in-One Models) are a series of profession computers that easily handle demanding computer tasks. Advanced state-of-the-art digital electronics and unique engineering concepts have been combined to form a truly exceptional and versatile family of computers.

Features of the Z-100 Series include:

- automatic selection on bootup of either an 8-bit processor (Intel 8085) or 16-bit processor (Intel 8088) allowing use of software for either.
- up to 3/4 megabyte of user addressable memory (RAM).
- an S-100 IEEE 696 standard bus with five slots for expansion.
- two RS-232 serial input/output ports.
- one parallel output port for Centronics-type devices.
- dynamically definable character set.
- high resolution pixel oriented (bit mapped) graphics for either color (8 colors) or monochrome (8 intensity levels) displays.
- a floppy disk controller that supports both 5.25-inch and 8-inch soft-sectored disk drives (single- or double-sided, single- or double-density, and 48- or 96-tpi, 5.25-inch drives).

These features, along with Zenith's commitment to quality, will give you a high-performance, dependable computer for many years to come.

GENERAL INFORMATION

System Description

The Z-100 Series All-in-One and Low-Profile Computers provides expandability; 8088, 8086, and 8080 code compatibility; and a 5MHz clock for computing power.

Expandability is provided through a 5-slot backplane on the main board. This allows you to expand your system with Heath/Zenith Data Systems peripherals and options or IEEE 696 standard S-100 cards from outside suppliers.

Code compatibility is provided through the use of an 8-bit processor (an Intel 8085) for 8080 code, and a 16-bit processor (an Intel 8088) for 8086 and 8088 code. The 8-bit processor allows you to use many of the large number of 8-bit code packages that run under the popular CP/M® operating system. The 16-bit processor allows you to utilize many of the 16-bit software packages that are rapidly becoming available for CP/M-86™ and MS™-DOS.

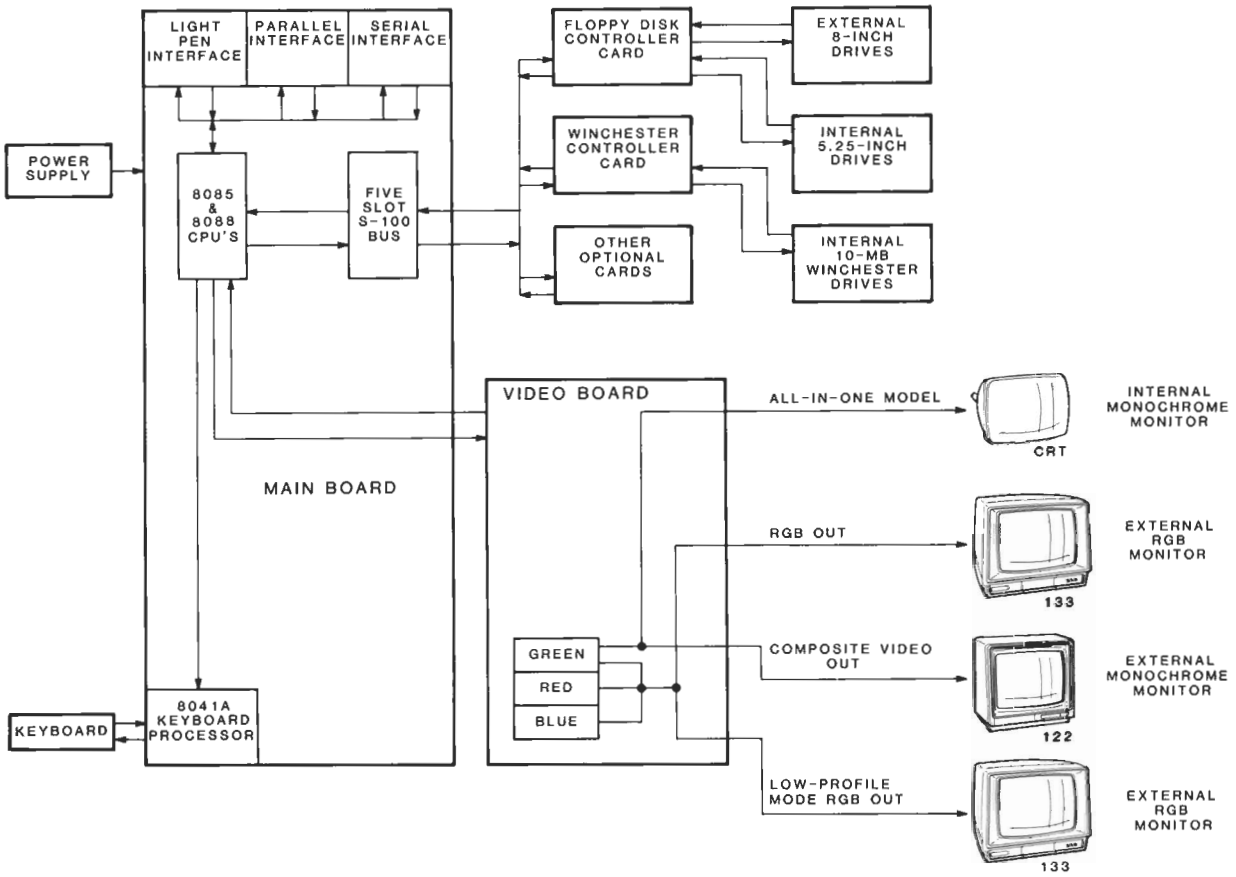
The 5 MHz clock provides high performance from both the 8088 and 8085 processors and will allow you to realize higher capabilities in input/output power than previously possible on limited 8-bit systems running under slower clocks.

System Modules

Refer to Pictorial 1-1 for the following discussion.

Power Supply

The power supply is an on line, switching power supply, providing +12VDC, −12VDC, +5VDC, and −5VDC. It is cooled by an internal fan and is protected from overvoltage, undervoltage, overcurrent, and overtemperature operation. This power supply is not serviceable.



Pictorial 1-1. System Block Diagram

GENERAL INFORMATION

System Description

Main Board

The main circuit board contains the two processors, an 8085 and an 8088, (CPU's—referred to as the master processors); the 5-slot backplane with an S-100 IEEE 696 bus; capacity for 3 banks of 64K devices for user memory, up to 192K; 8041A keyboard processor and connections for the keyboard; two RS-232 serial interfaces and connectors, one parallel interface and connector, and interface with the video board.

The CPU's control the timing, addressing, and generation of control signals for the computer. In addition, switches and jumpers on the main board control autobooting, vertical scan frequency, interfacing for the serial ports, and PROM size (8, 16, or 32K × 8).

Temporary master processors on cards plugged into the backplane slots can directly access the memory and peripheral ports of the system. They cannot, however, access the interrupt controllers for the two master processors, the high order address latch, or the processor swap port (these can only be accessed by the master processors on the main board —the 8085 and 8088).

128K of user memory on the main board is supplied in the standard configuration, however 192K is supplied for some systems, which is required for Winchester operation and some application packages. Associated circuitry provides parity checking and refresh cycles.

Video Circuit Board

The Z-100 series computers support a powerful bit-mapped video system, requiring a minimum of one bank of 32K for video memory. The video circuit board has the capacity for up to three banks (one each for red, green, and blue) of 32K or 64K memory devices. The video board interfaces with the main board and contains the CRT controller (CRTC) and output facilities for both composite monochrome monitors and RGB color monitors.

Jumpers provide flexibility in selecting memory device types, although they may not be mixed, and RGB or monochrome operation. In addition, if 32K of 64K devices are used, the board has provisions for addressing the upper or lower 32K.

The video board is directly accessible from the S-100 bus and may controlled by either temporary or master processors. The CRTC, video control bits, and video RAM are all accessible from the S-100 bus and are compatible with it. However, the board is not an S-100 board and does not meet S-100 standards for signal interfacing or power supply requirements.

Floppy Disk Controller

The floppy disk controller is on a card that occupies one of the five S-100 slots. It conforms to IEEE-696 standards for S-100 cards and provides the necessary read/write and control signals for up to four 5.25-inch and four 8-inch floppy disk drives. Drive types may be mixed and are dependent upon the operating system for control. Note: Standard Z-DOS, CP/M-85, and CP/M-86 operating systems, as supported by Zenith Data Systems, are configured to support only two of each drive size. If additional drives are required, the operating systems will have to be modified by the user.

GENERAL INFORMATION

System Description

Winchester Disk Controller

The optional Winchester disk controller is on a card that also occupies one of the five S-100 slots. It conforms to IEEE 696 standards for S-100 cards. The data separator for the Winchester system is on a separate circuit board and is mounted on the Winchester disk drive itself. The two cards provide the necessary read/write and control signals for up to two Winchester drives. Note that Zenith Data Systems supports operating system software for only one Winchester drive at this time for single user installations.

Other Options

Other optional S-100 cards are available from Zenith Data Systems. They include the NET-100 Z-LAN™ network card and interface software, the Z-204 multiport input/output card (available with or without ring detect), and the Z-205 memory card (with a capacity for 256K additional RAM memory).

In addition, cards from other suppliers may be added that are IEEE 696-compatible. Note that neither Zenith Data Systems nor Heath support nor recommend the use of any of these cards.

Disassembly

There are a number of versions of both the Low-Profile and All-in-One Z-100 Series available. The variations in the configurations are limited to 5.25-inch drive size (both full-sized and half-height versions are available) and whether or not the optional Winchester disk system is installed in the computer.

In addition, optional cards can be added to accommodate additional memory, additional input/output ports, and the Zenith Local Area Network (Z-LAN).

When you are disassembling your system, keep in mind there various options and if installed, draw a chart of the cable connections of the S-100 cards in your particular system.

NOTE: If you have a Winchester system, make sure that the drive is in the SHIP position. See your *Z-100 User's Manual Winchester Supplement* for instructions.

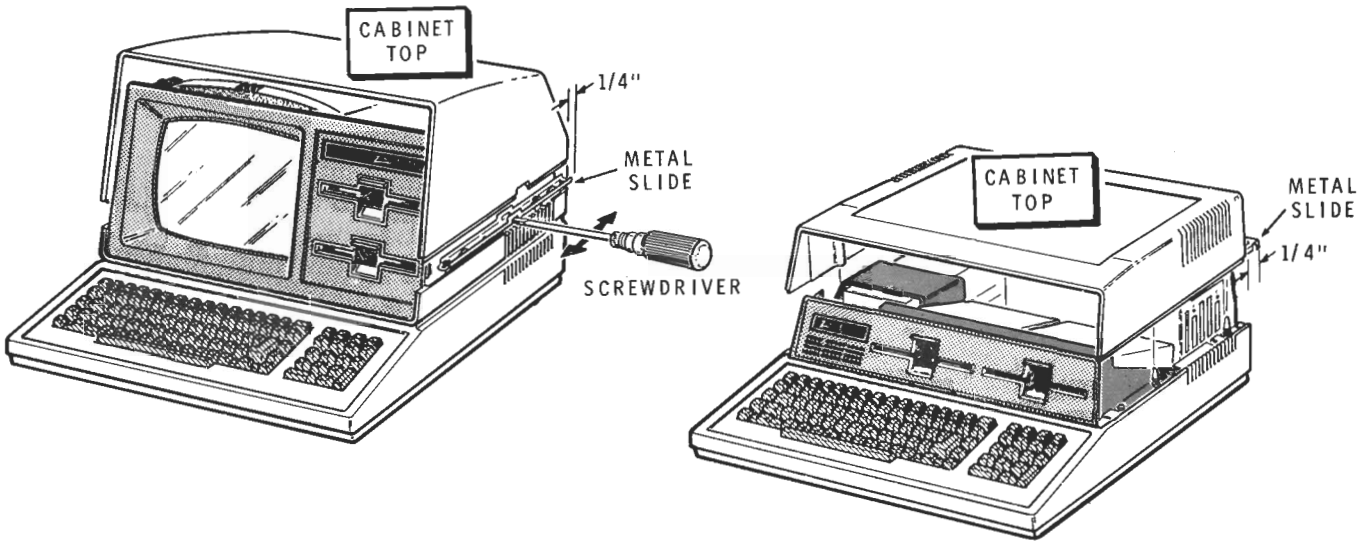
Cabinet Removal

Before proceeding with disassembly, disconnect all line cords to your computer and its peripherals.

GENERAL INFORMATION

Disassembly

Refer to Pictorial 1-2 and move the metal slides to the rear approximately 1/4-inch as shown. Carefully lift off the cabinet top and set it to one side. (On the All-in-One models, you will have to use a flat-bladed screwdriver as illustrated in the pictorial.



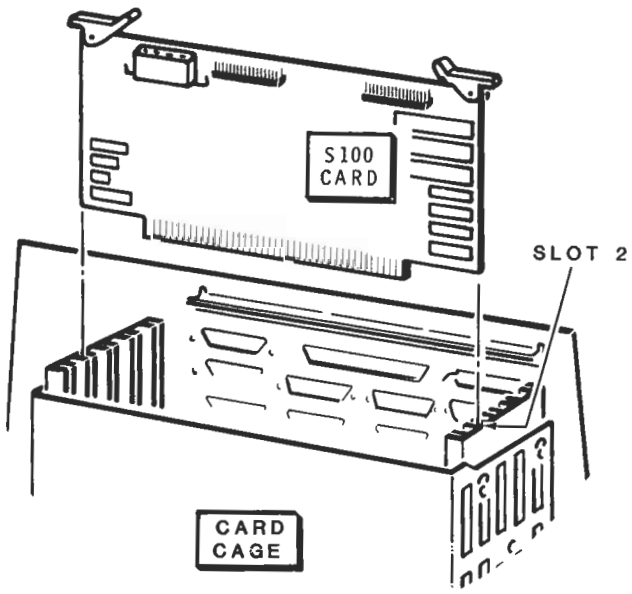
Pictorial 1-2. Cabinet Removal

Card Removal

Refer to Pictorial 1-3. The various cards in your computer can be removed as your needs dictate. However, be aware that you will occasionally have to remove cables from several different cards to remove one card.

For instance, if you want to remove the floppy disk controller card and you have a Winchester card installed *to the back of it* (as viewed from the front of the computer, you will have to remove the cables going from the Winchester card to the drive. Likewise, if you are removing the Winchester controller card (for installation of the jumper for PREP operation), you may have to remove one of the two cables going from the floppy disk controller card.

Cards may be removed by simultaneously pivoting up both of the card lifters as illustrated in the pictorial, unplugging any cables (including those that may be routed over the card you are removing), and then lifting the card up out of the computer.



Pictorial 1-3. Card Removal

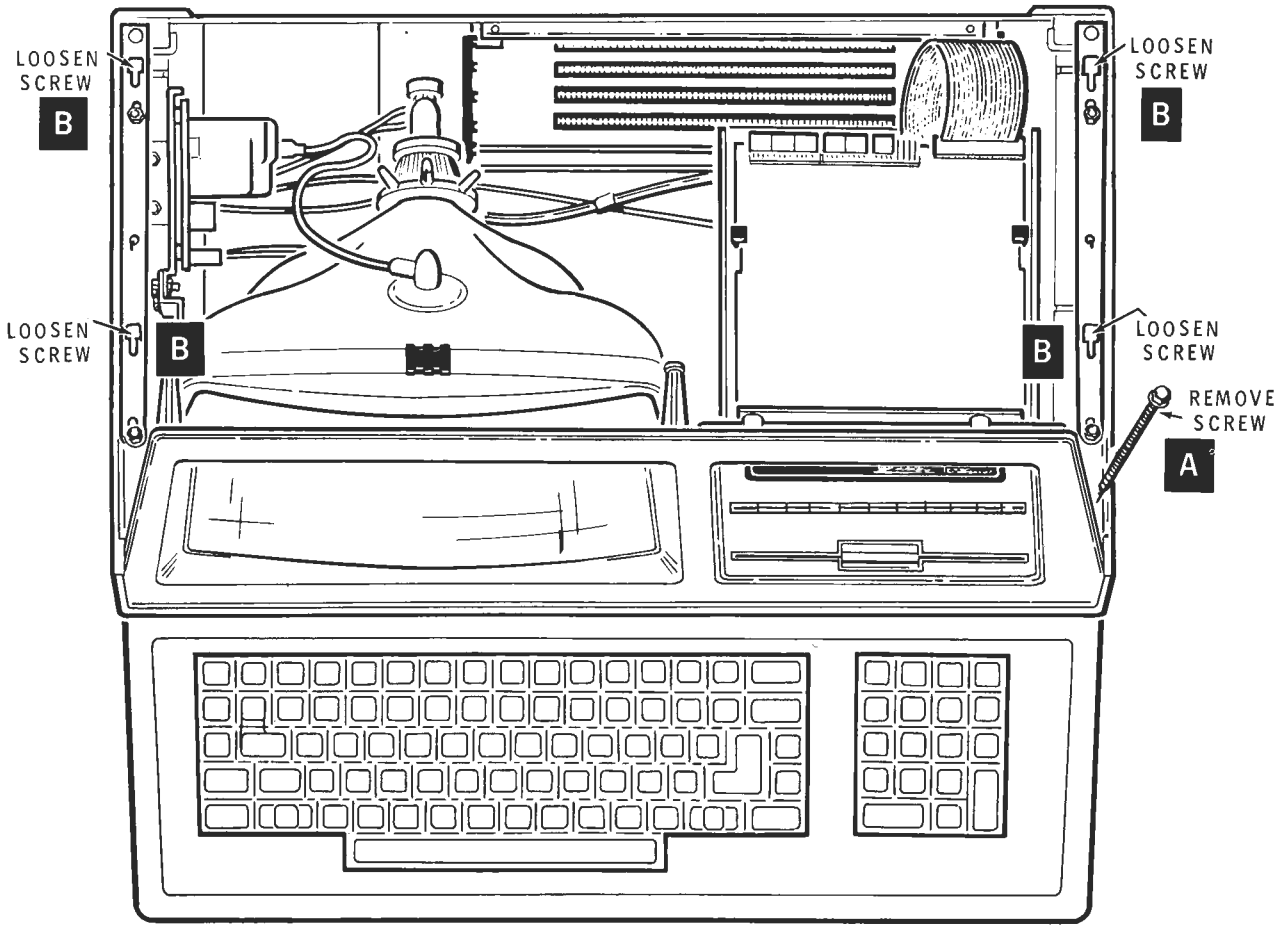
GENERAL INFORMATION

Disassembly

Display and Disk Drive Assembly (All-in-One Computer)

Refer to Pictorial 1-4.

☐ Remove screw A and completely loosen the four B screws (these last four may be accessed through holes in the cabinet slides. Lift the display and disk drive assembly up and forward a short distance.

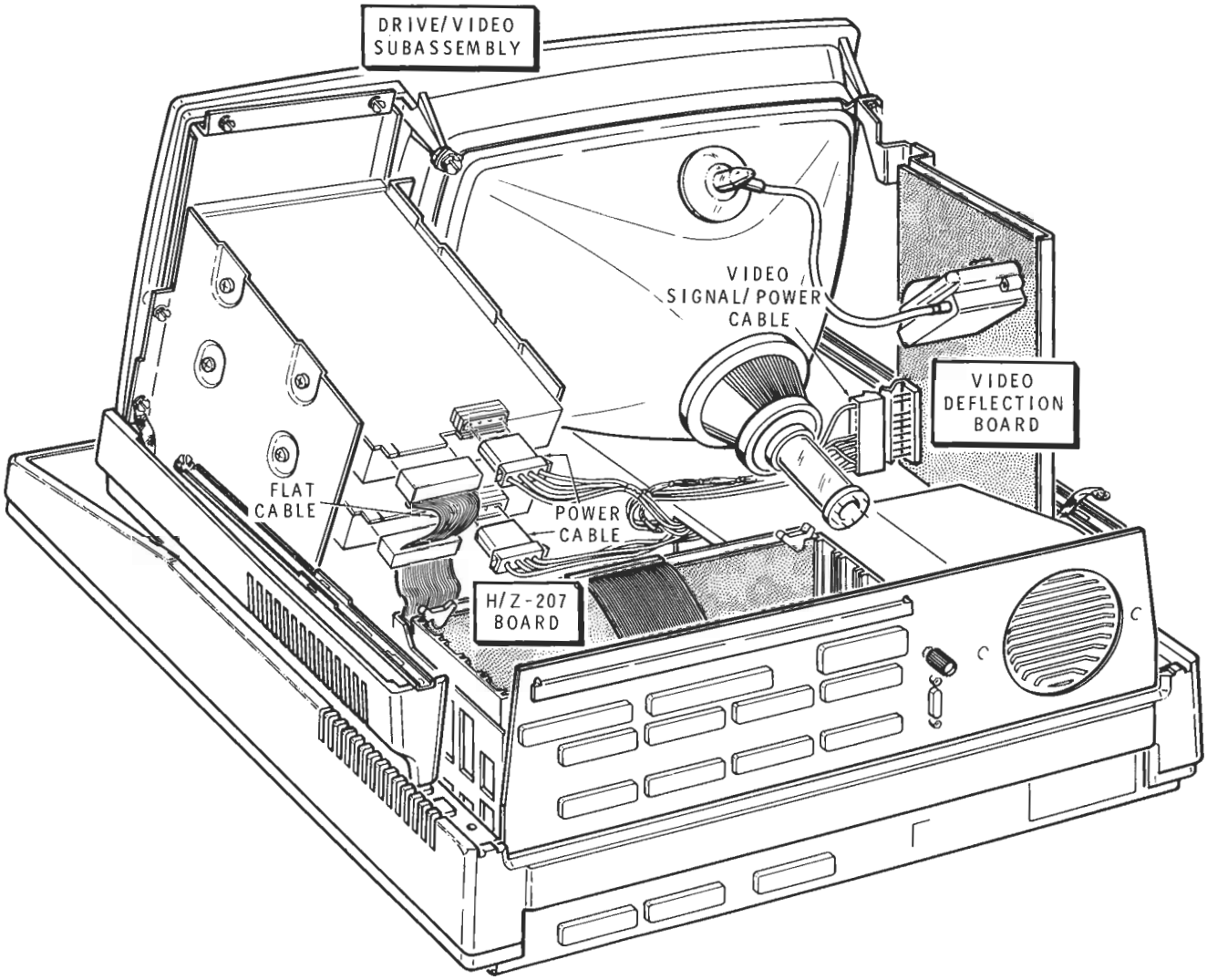


Pictorial 1-4. Display and Disk Drive Assembly Removal

Disassembly

☐ Floppy Disk Systems only; refer to Pictorial 1-5 and remove:

- the flat cable from the floppy disk controller card,
- the power supply cable(s) at the drive(s), and
- the video signal/power cable on the video deflection board.



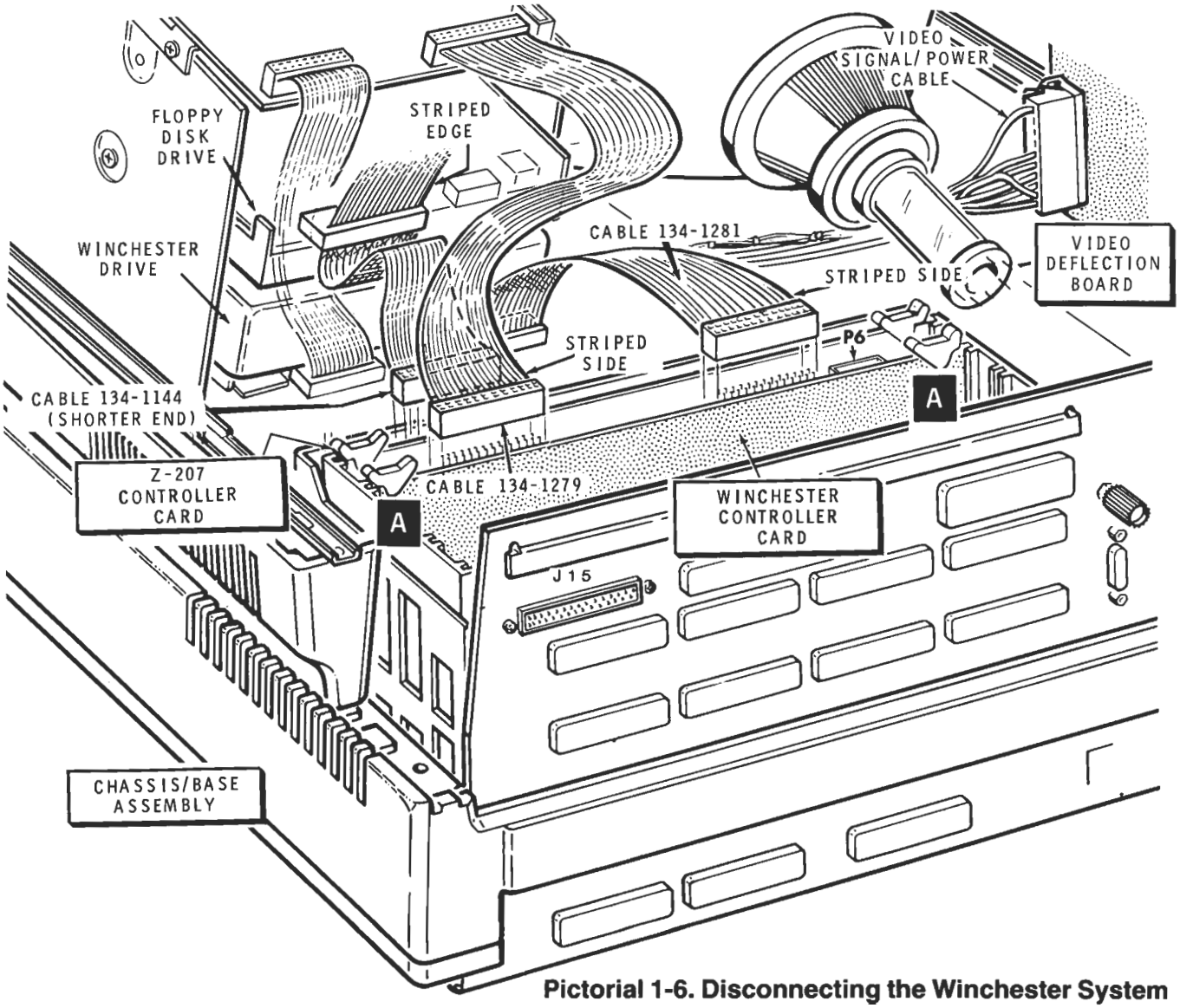
Pictorial 1-5. Disconnecting the Floppy Disk Drives

GENERAL INFORMATION

Disassembly

☐ Winchester Disk Systems only; refer to Pictorial 1-6 and remove:

- the two flat cables (134-1279 and 134-1281) from the Winchester controller card,
- the flat cable (134-1144) from the floppy disk controller card,
- the power cable from the Winchester controller card,
- the power supply cables from the drives, and
- the video signal/power cable on the video deflection board.



Pictorial 1-6. Disconnecting the Winchester System

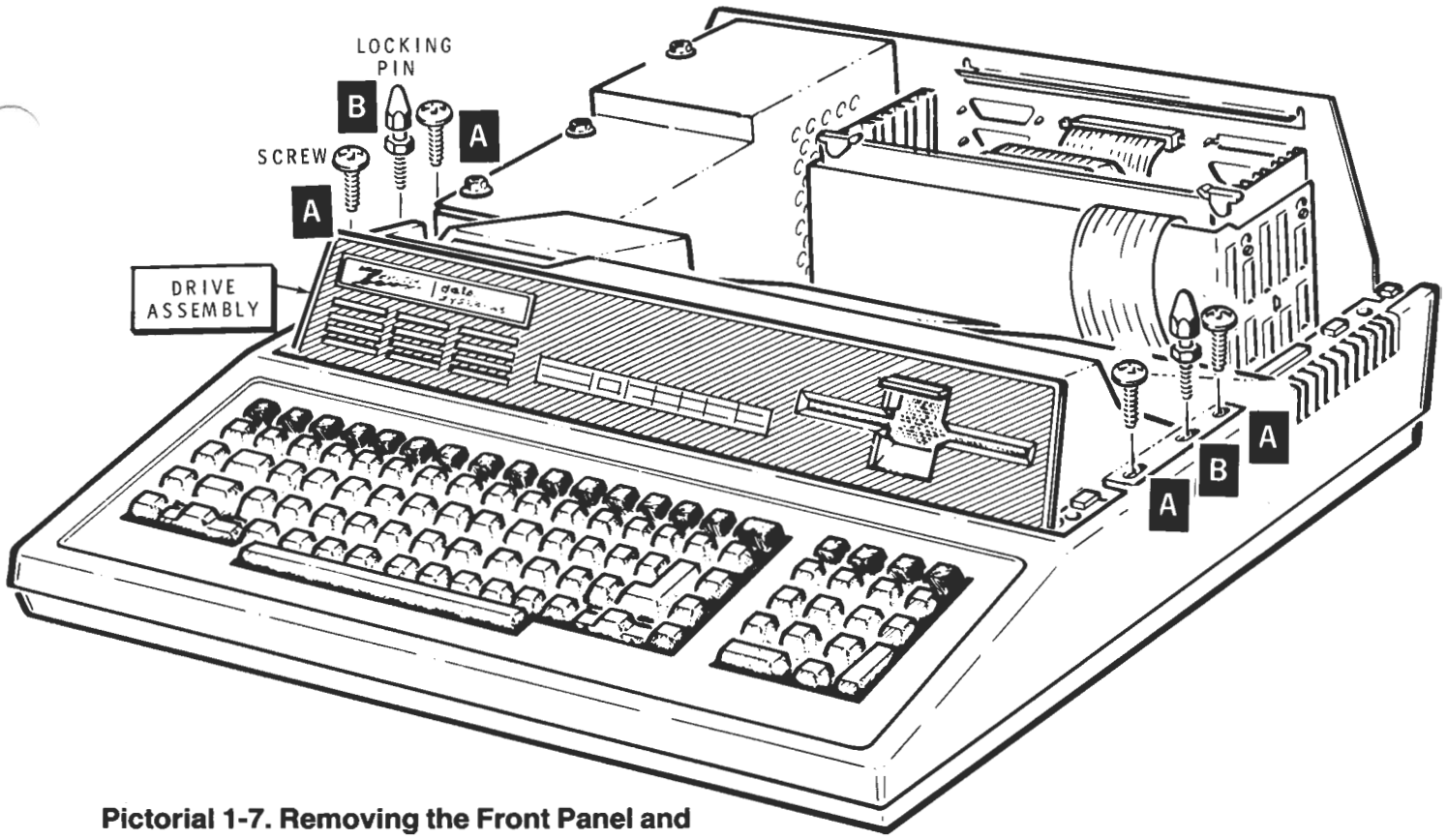
Disassembly

Low-Profile Front Panel and Disk Drive Assembly

Refer to Pictorial 1-7.

☐ Remove the four screws at A and two locking pins at B.

☐ Lift the front panel and disk drive assembly out of the computer and to the front a short distance.



Pictorial 1-7. Removing the Front Panel and Disk Drive Assembly

GENERAL INFORMATION

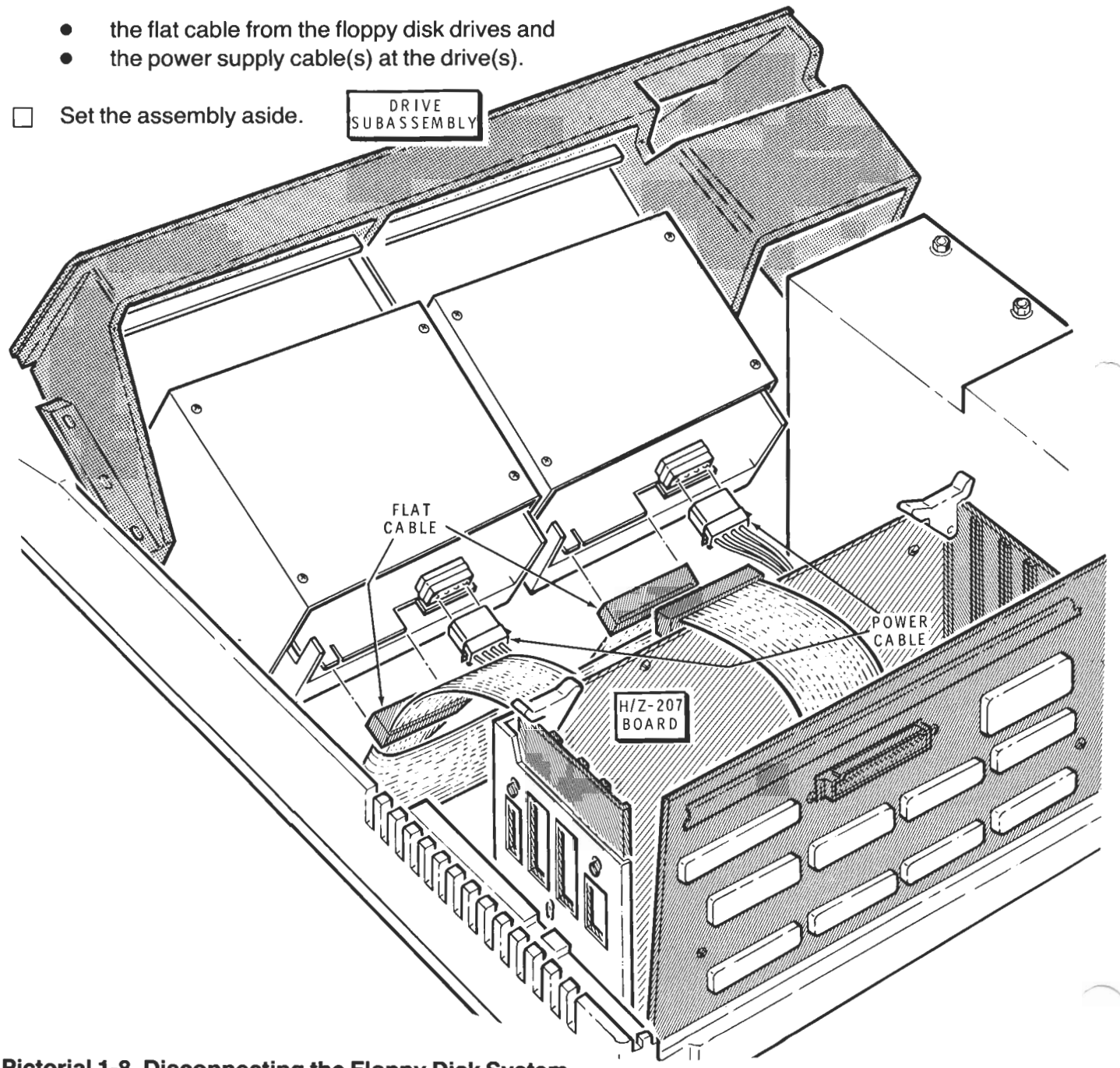
Disassembly

Refer to Pictorial 1-8.

☐ Floppy Disk Systems only; remove:

- the flat cable from the floppy disk drives and
- the power supply cable(s) at the drive(s).

☐ Set the assembly aside.



Pictorial 1-8. Disconnecting the Floppy Disk System

GENERAL INFORMATION

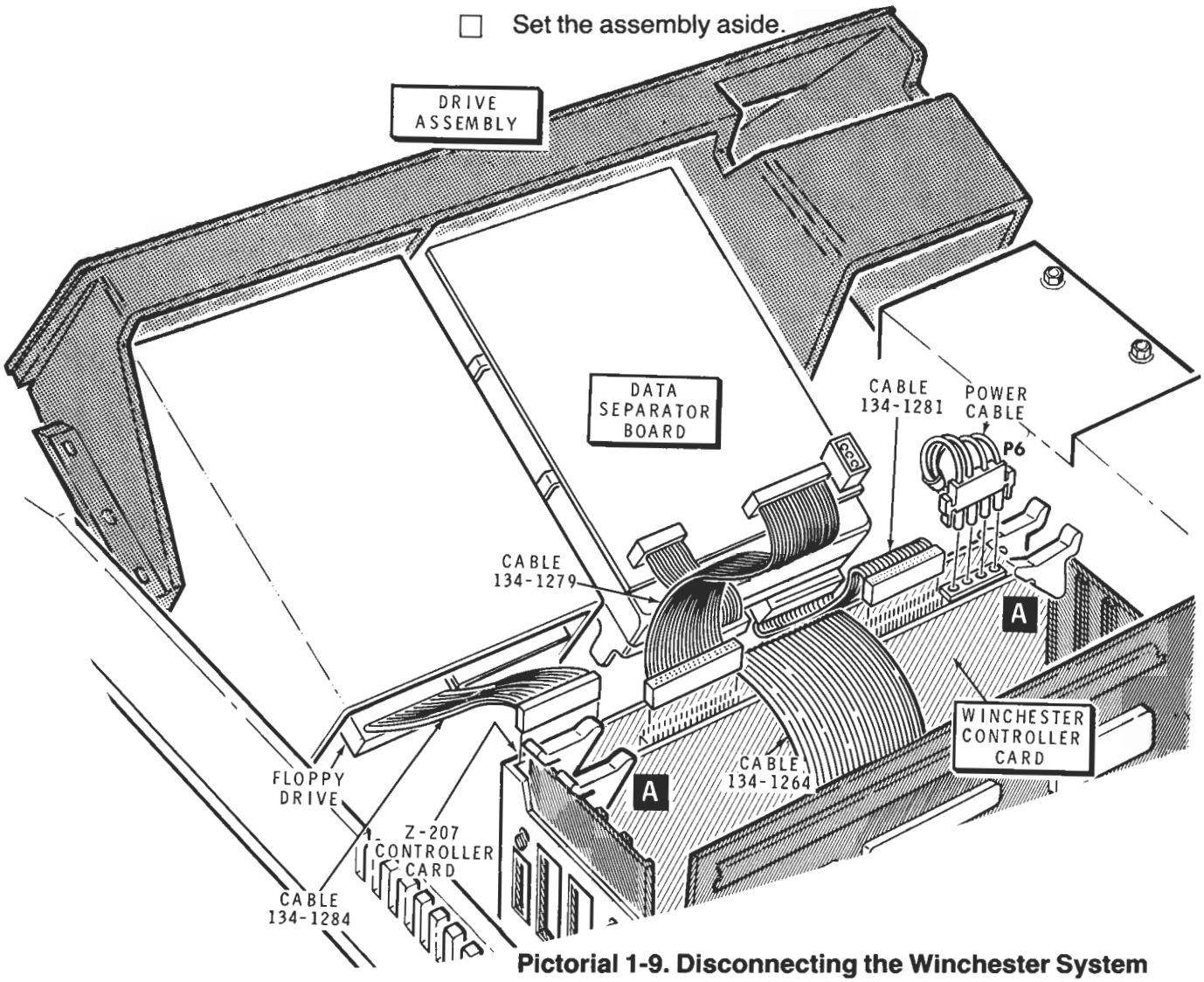
Disassembly

Refer to Pictorial 1-9.

☐ Winchester Disk Systems only; remove:

- the two flat cables (134-1279 and 134-1281) from the Winchester controller card,
- the power cable from the Winchester controller card,
- the flat cable (134-1284) from the floppy disk controller card, and
- the power supply cables at the drives.

☐ Set the assembly aside.



Pictorial 1-9. Disconnecting the Winchester System

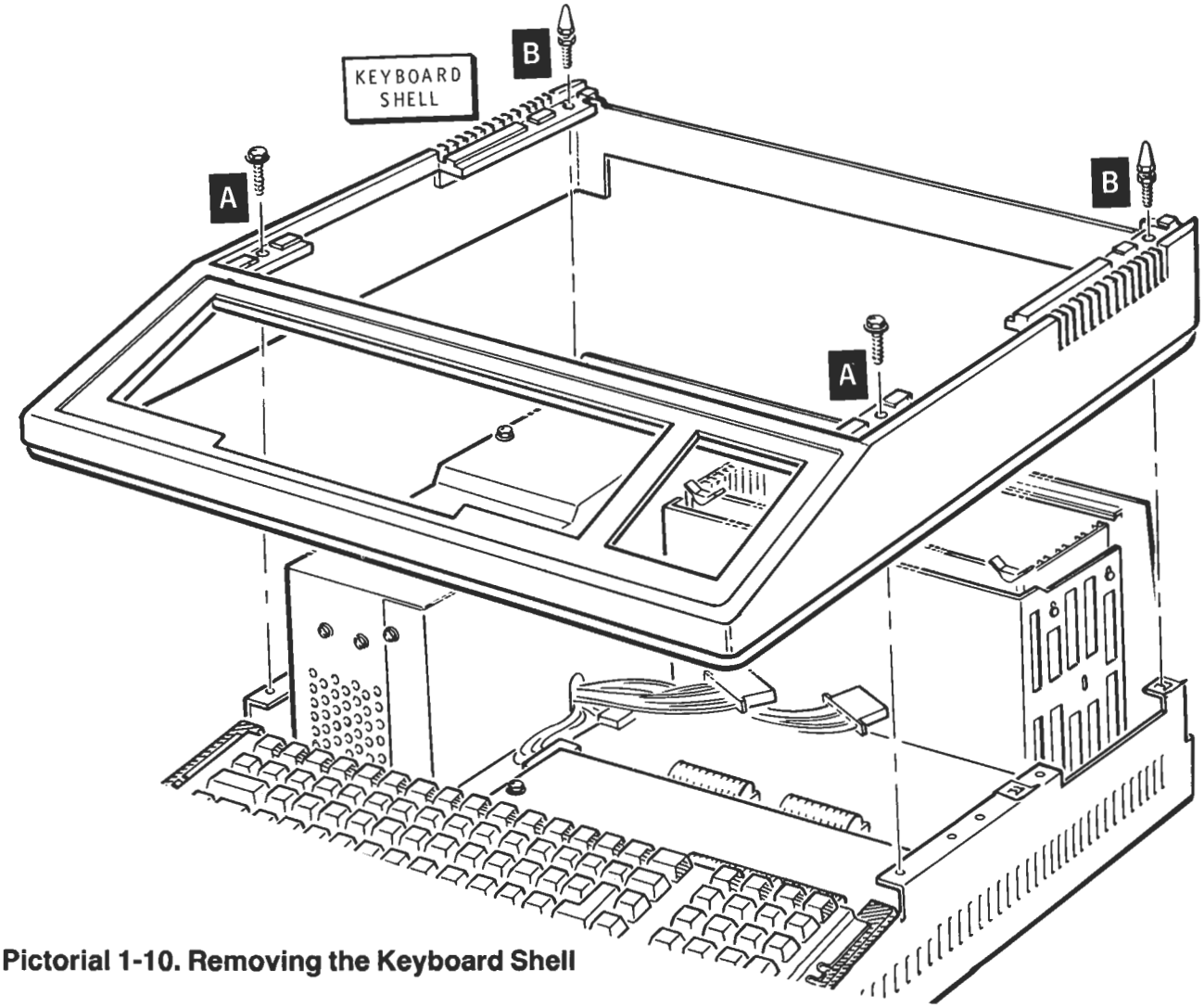
GENERAL INFORMATION

Disassembly

Keyboard

Refer to Pictorial 1-10.

- ☐ Remove the two screws at A from near the top of the keyboard.
- ☐ Low-Profile models only; remove the two locking pins at B from near the rear of the computer.
- ☐ Lift off the keyboard shell. Set the shell to one side.

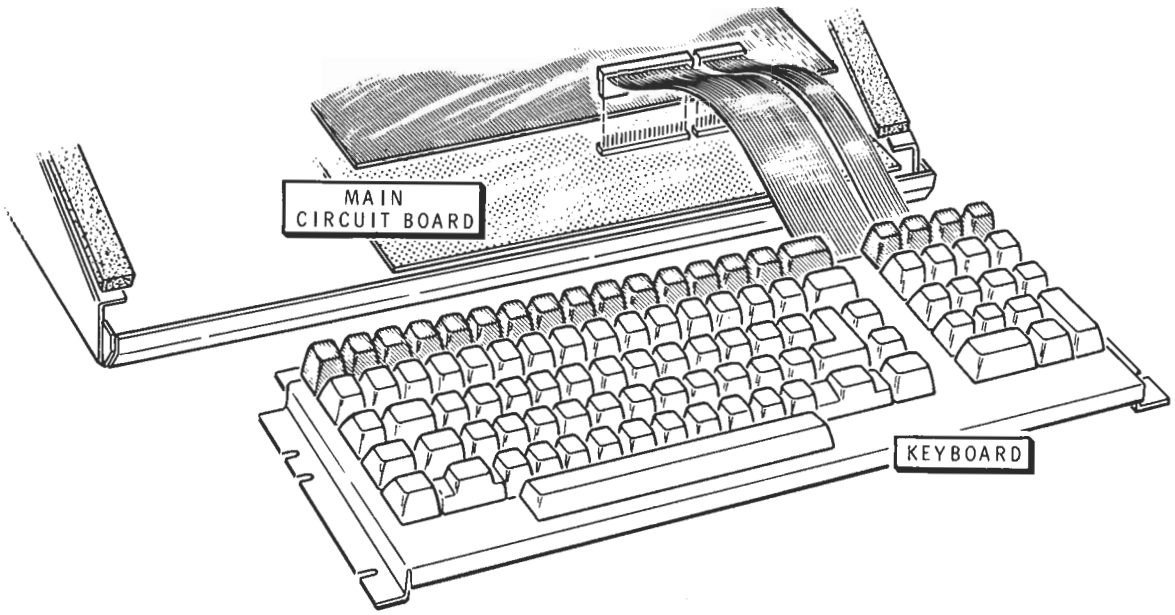


Pictorial 1-10. Removing the Keyboard Shell

Disassembly

Refer to Pictorial 1-11.

☐ Move the keyboard forward and unplug the two cables from the main board. Set the keyboard to one side.



Pictorial 1-11. Removing the Keyboard

GENERAL INFORMATION

Disassembly

Power Supply

Refer to Pictorial 1-12.

NOTE: Your power supply may look different than the one illustrated.

- ☐ Unplug remaining power cables.
- ☐ Remove the four screws at A from the rear panel as illustrated.
- ☐ Remove the two screws at B from the front bottom of the power supply that hold it to the base.
- ☐ Lift the power supply out of the computer and set it to one side.

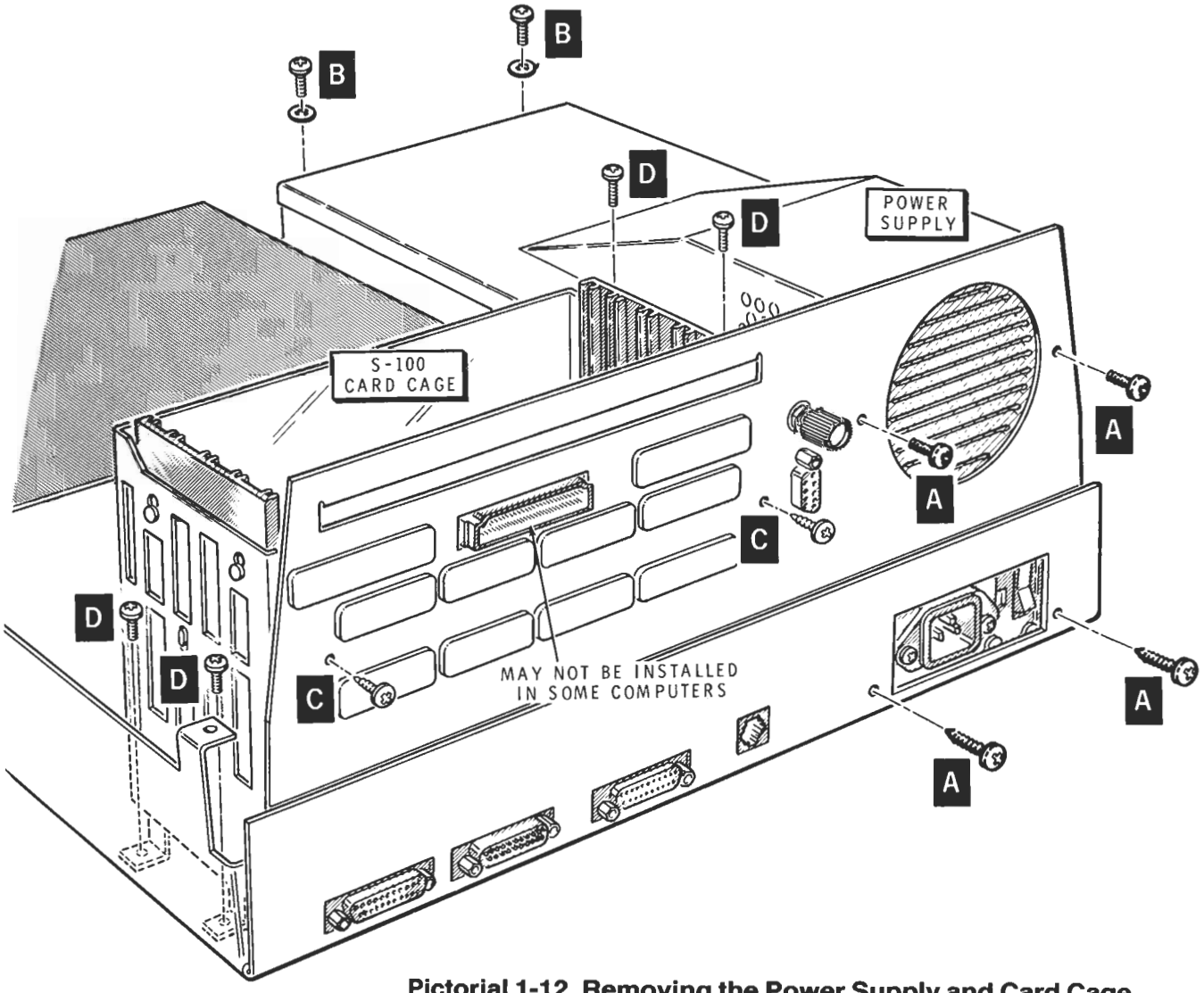
WARNING: There are no user-serviceable parts inside your power supply. Never open it up or break the seal; with a line cord attached, there are lethal voltages present!

Card Cage

- ☐ Disconnect any remaining cables to cards in the card cage. Note their positions; because of the large variety of options available and new or planned products, no illustrations are provided in this manual for reconnecting these cables.

Disassembly

- ☐ Remove all cards from the card cage and set them to one side.
- ☐ Remove the two screws at C from the rear panel as illustrated.
- ☐ Remove the four screws at D from the base as illustrated.
- ☐ Remove and set the card cage to one side.



Pictorial 1-12. Removing the Power Supply and Card Cage

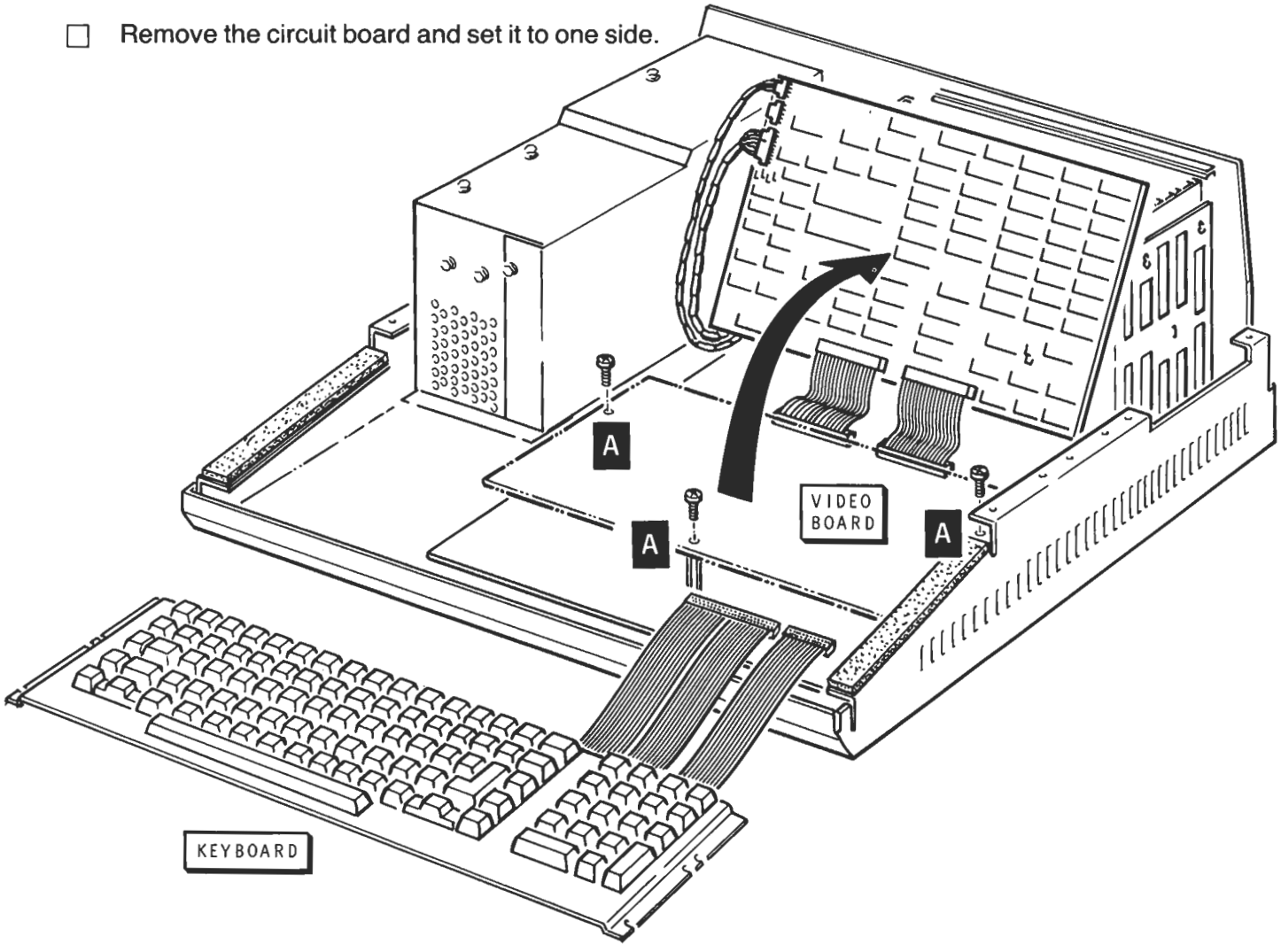
GENERAL INFORMATION

Disassembly

Video Logic Circuit Board

Refer to Pictorial 1-13.

- ☐ Remove the three screws holding the board to the three hex mounting spacers.
- ☐ Unplug the two cables from the main board.
- ☐ Remove the circuit board and set it to one side.



Pictorial 1-13. Removing the Video Logic Board

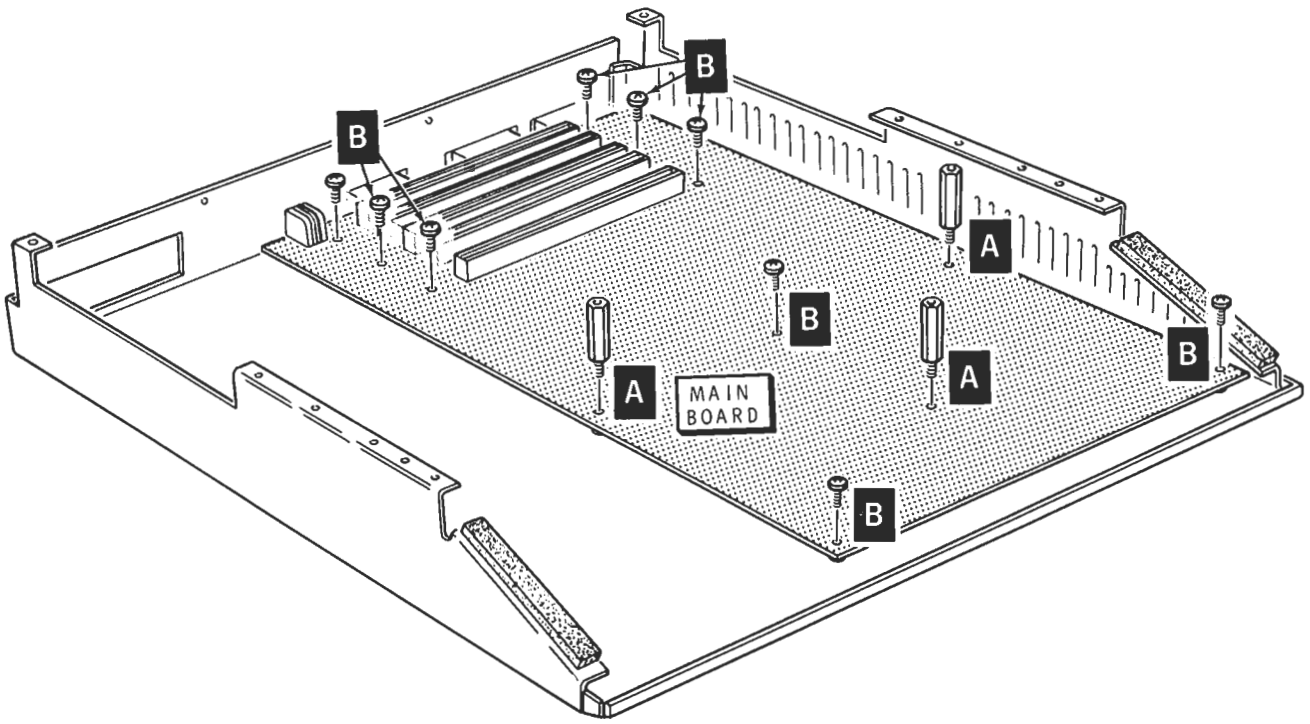
Disassembly

Main Board

Refer to Pictorial 1-14.

- ☐ Remove the three hex mounting spacers at A from the main board.
- ☐ Remove the nine screws at B from the main board.
- ☐ Remove the main board and set it to one side.

This completes the disassembly of the modules of your computer. The next section covers disassembly of the disk drive modules.



Pictorial 1-14. Removing the Main Board

GENERAL INFORMATION

Disassembly

Disk Drive Modules

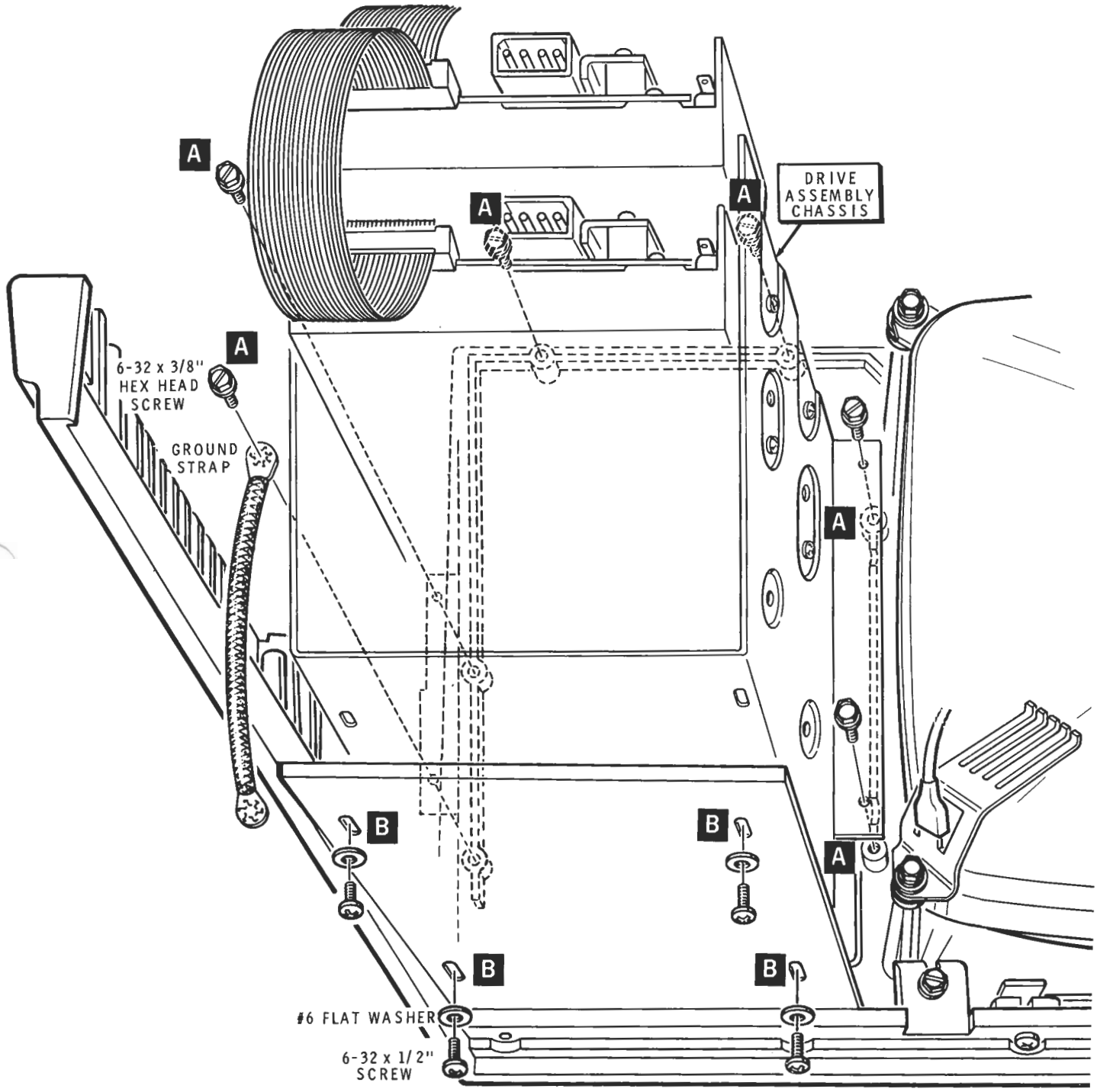
There are several different configurations of disk drives for your computer. These include units with one or two floppy disk drives, one floppy disk drive and one Winchester drive, and similar modules with half-height floppy disk drives.

All-in-One Models

Refer to Pictorial 1-15. Note that this pictorial illustrates a two-drive half-height module; the following instructions apply equally to all configurations of the All-in-One computer — full-sized floppy disk, half-height floppy disk, and Winchester versions.

- ☐ Remove the four screws and spacers at B.
- ☐ Remove the six screws at A. Note the ground strap placement.
- ☐ Remove the drive assembly chassis from the display and disk drive assembly.
- ☐ Set the display assembly to one side.

Disassembly



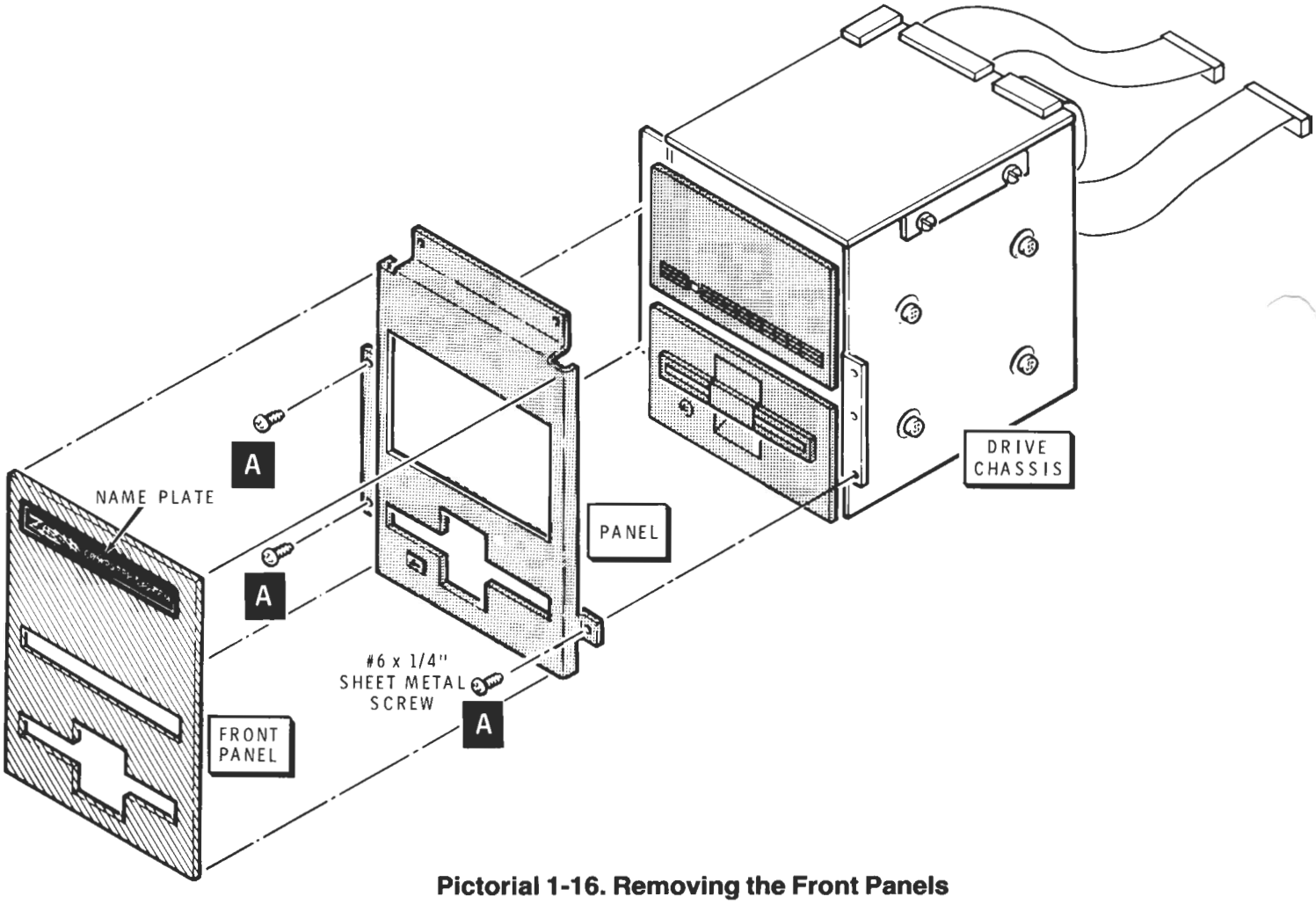
Pictorial 1-15. Removing the Disk Drive Assembly

GENERAL INFORMATION

Disassembly

Refer to Pictorial 1-16. This pictorial illustrates a Winchester and full-sized floppy disk system. Your system, whether it is a half-height or floppy disk only version will be similar.

☐ Remove the three screws at A and remove the front panel and panel from the assembly.



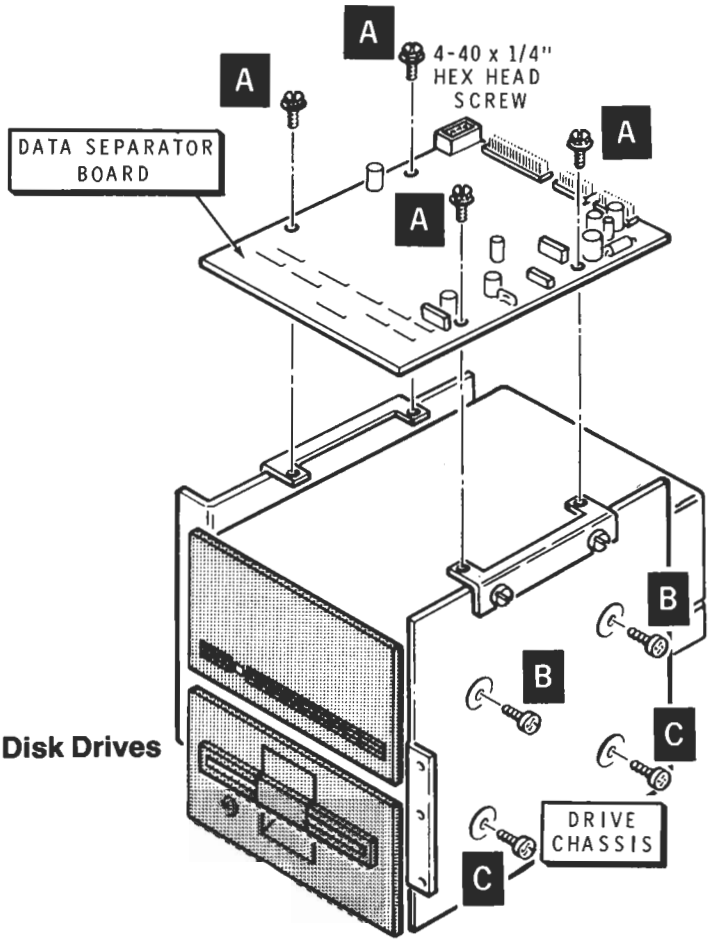
Pictorial 1-16. Removing the Front Panels

Disassembly

Winchester Systems

Refer to Pictorial 1-17.

- ☐ Remove the data separator cable assembly 134-1380 from the data separator board.
- ☐ Remove the four screws at A and remove the data separator board; set it to one side.
- ☐ Full-sized floppy disk drives only; remove the four screws at B and remove the Winchester disk drive.
- ☐ Full-sized floppy disk drives only; remove the four screws at C and remove the floppy disk drive.



Pictorial 1-17. Removing the Disk Drives

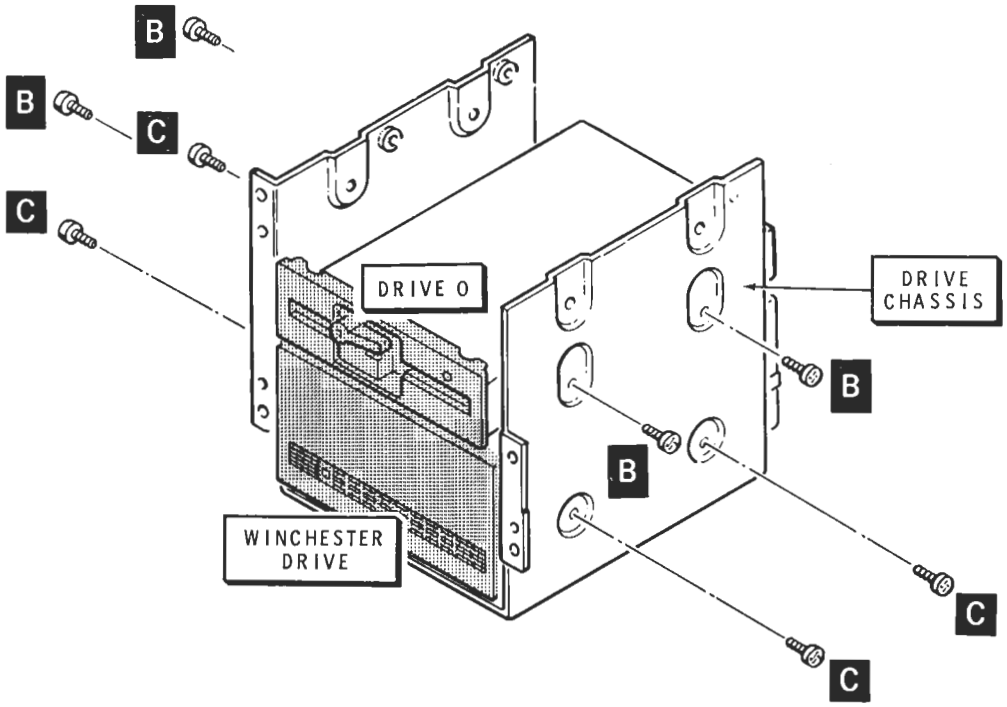
GENERAL INFORMATION

Disassembly

Refer to Pictorial 1-18.

☐ Half-height floppy disk drives only; remove the four screws at B and remove the floppy disk drive.

☐ Half-height floppy disk drives only; remove the four screws at C and remove the Winchester disk drive.



Pictorial 1-18. Removing the Disk Drives

Low-Profile Models

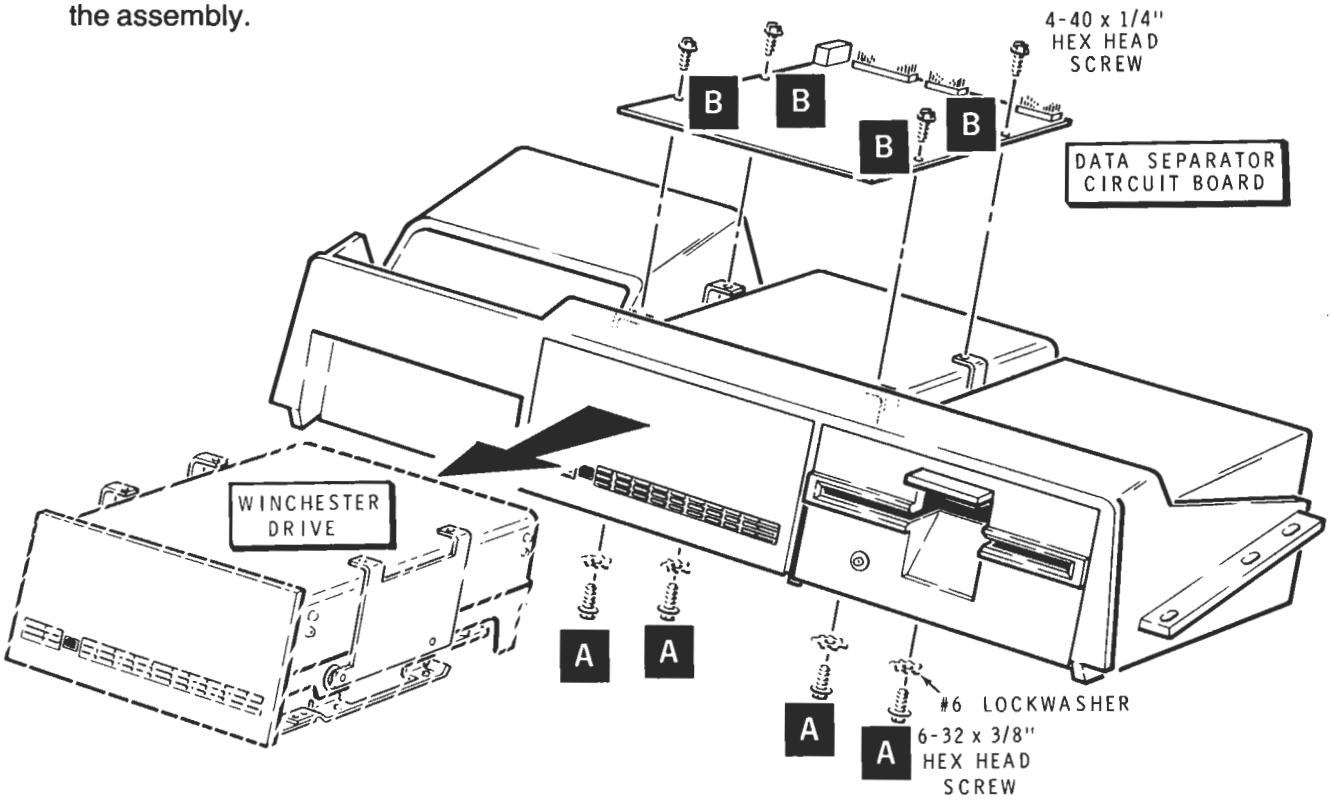
☐ Get the front panel and disk drive assembly that you set to one side earlier.

☐ Carefully remove the front panel from the front of the assembly. Set it to one side where the tacky side will not be contaminated by dust, lint, paper, or other objects.

Refer to Pictorial 1-19.

☐ Winchester versions only; remove the four screws at B and remove the data separator board.

☐ Winchester versions only; remove the four screws at A and carefully slide the Winchester drive out the front of the assembly.



Pictorial 1-19. Removing the Winchester Drive

GENERAL INFORMATION

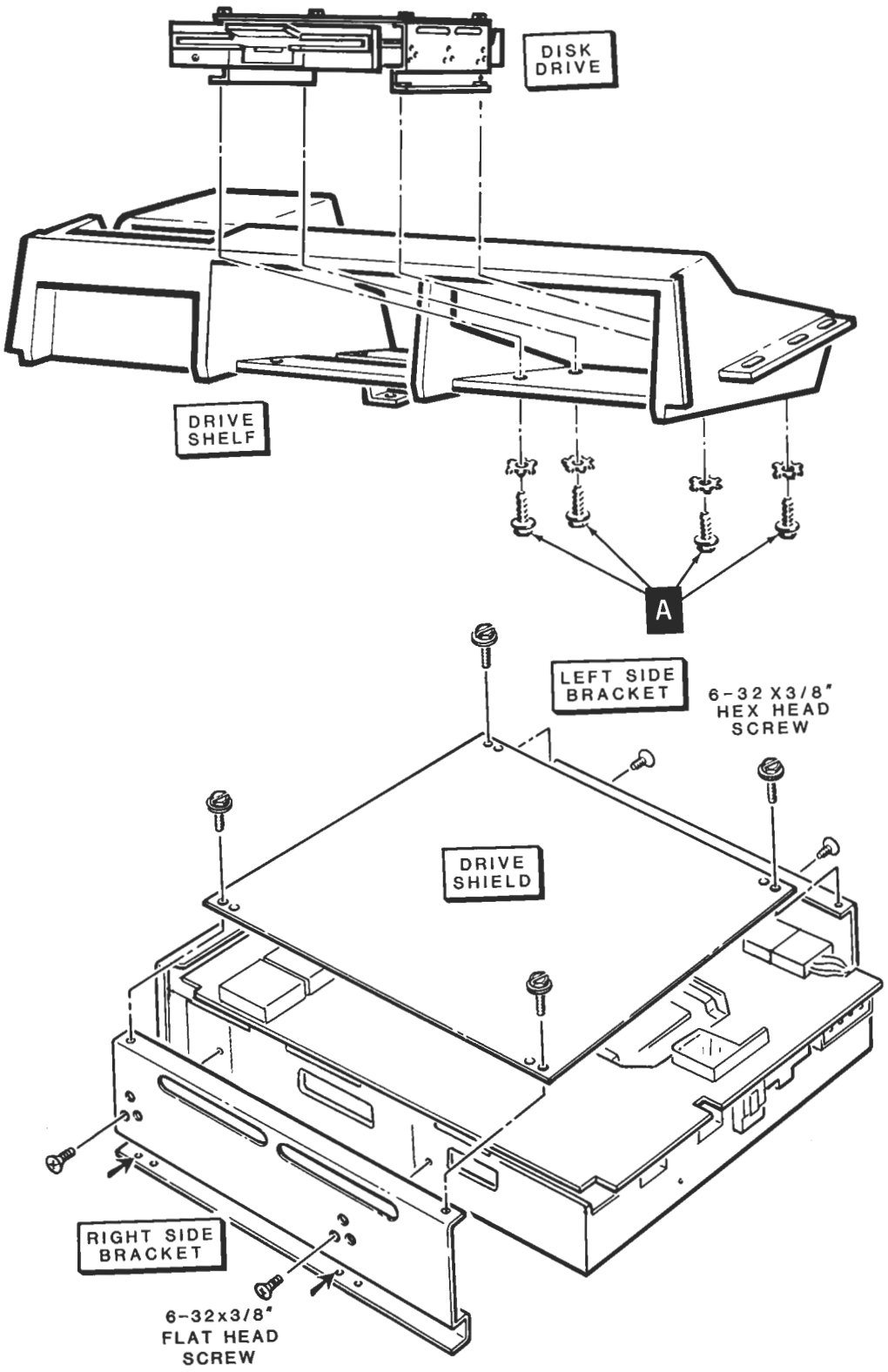
Disassembly

Refer to Pictorial 1-20. This pictorial illustrates removal of a half-height drive from the drive shelf. Removal of a full-sized drive is similar.

- ☐ Remove the four screws at A and slide the floppy disk drive out the front of the assembly.
- ☐ Half-height versions only; remove the four screws holding the drive shield to the left and right side brackets.
- ☐ Half-height versions only; remove the two flat head screws that hold each side bracket to the drive. Note the placement of the mounting screws in the side bracket; the position and holes used will vary according to the drive used in your system.
- ☐ If your system has two floppy disk drives, the second drive may be removed in a similar manner to the first.

This completes the disassembly section of your manual. Parts are identified in the various parts lists through this and other technical manuals published by Zenith Data Systems. A complete service manual is also available from Heath replacement parts or your local dealer.

Disassembly



Pictorial 1-20. Removing the Floppy Disk Drives

Main Board

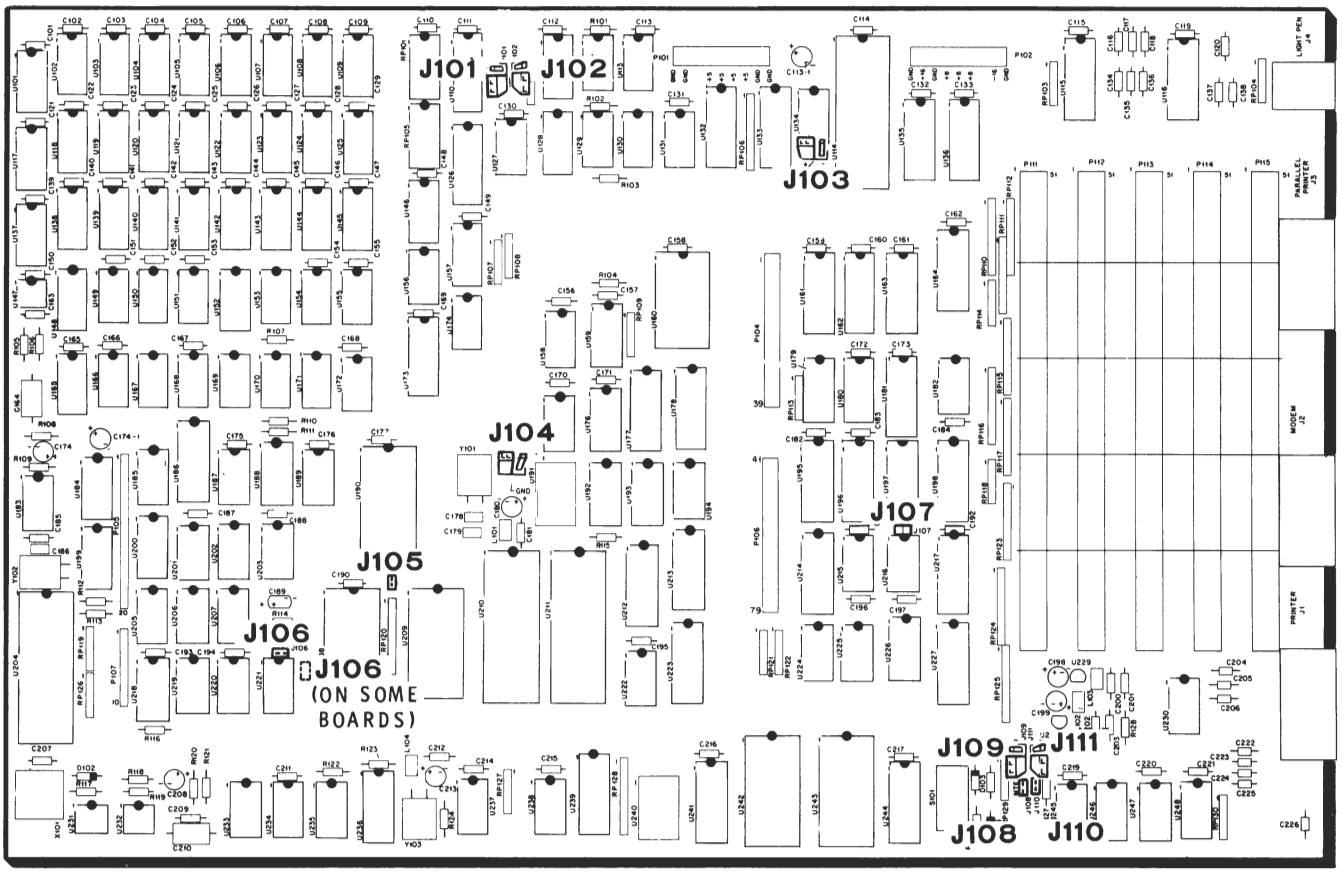
DESCRIPTION

The main board is the permanent bus master unit in the S-100 bus system and contains two microprocessors, an 8085 and an 8088. Both operate at 5 MHz. The 8088 has a 16-bit internal architecture that interfaces to an 8-bit external architecture, while the 8085 is a pure 8-bit processor.

The main board also contains up to 32k bytes of ROM, and up to 192k bytes of RAM with parity. There are two serial ports, a parallel printer port, a light pen port, a keyboard, and a timer. All of these ports are accessible from the S-100 bus.

The five-slot S-100 bus is located on the main board. This bus meets the proposed IEEE-696 definition of an S-100 bus.

The main board itself is not an S-100 card, although it meets the signal interface requirements of an S-100 card.



Pictorial 2-1
Main Circuit Board

USER OPTIONS AND JUMPERS

Refer to Pictorial 2-1 as you read the following information.

Switch S101

DIP switch S101 selects the following functions during power-up or master reset. Set the switches for your system and preferences.

Switch S101, Section	Description
0 1	Default boot device*
2	1 = Auto boot, 0 = Manual boot
3 4 5 6	not used
7	0 = 60 Hz, 1 = 50 Hz; for video vertical scan frequency.

Sections 0, 1, and 2 should be set to reflect the type of drive that the system is to be booted from:

Switch Section 2	1	0	Device Type
0	0	0	5-1/4" floppy disk drive (internal)
0	0	1	8" floppy disk drive (external)
0	1	0	5" Winchester disk (internal)

USER OPTIONS AND JUMPERS

Circuit Board Jumpers

The main board circuit board jumpers perform the following functions:

J101 — Selects whether +5VDC or address line BA14 is applied to pin 27 of the PROM. The position shown has +5VDC connected to pin 27 for an 8K × 8 or 16K × 8 PROM. Move the jumper to the other position to use a 32K × 8 EPROM.

J102 — Same as J101 except for address line BA13 and pin 26 of the PROM. The position shown is for using an 8K × 8 EPROM. Move the jumper to the other position to use a 16K × 8 or a 32K = 8 EPROM.

J103 — Controls which transition of the light pen strobe (LTPNSTB) will cause a light pen interrupt. The position shown causes an interrupt on the negative-going edge. It is properly jumpered for operation with a light pen that causes a negative pulse during a "hit."

J104 — No jumper is needed at this position. A foil trace connects the indicated two pins as shown. If the foil is cut and a jumper is installed in the other position, an NMI (TRAP for the 8085) will be generated when the S-100 power fail signal (PWRFAIL*) is active.

J105 — No jumper is needed at this position. If a jumper is installed, the TEST input to the 8088 will be grounded. Otherwise, this input is high.

J106 — For factory test use only.

J107 — No jumper is needed at this position. A foil trace connects the two pins together. If the foil is cut, the main board will not provide the S-100 MWRT signal. Currently, the main board does provide this signal to the S-100 bus.

USER OPTIONS AND JUMPERS

J108 — No jumper is presently used at this position. If a jumper plug is installed, serial port B will generate an interrupt when the transmitter is empty (TXEMT active) in addition to its normal interrupts.

J109 — This jumper connects serial port A DCD input to either ground or RTS from the connector. It is normally set in the mode shown that connects DCD to RTS.

J110 — Same as J108, but for serial port A.

J111 — This jumper connects the serial port A CTS line to either ground or RTS from the serial connector. It is normally set in the position shown, which connects the CTS line to ground.

PROGRAMMING INFORMATION

The information in this section concerns the main board only and is meant to be used by the experienced programmer. Programming for the entire system is contained in "Programming Data" toward the end of this manual.

Port Addresses

The following port addresses are for devices located on the main board. A more complete list can be found in "Programming Data."

Device Name	Port Address (HEX)
DIP Switch	FF
Processor Swap	FE
High Address Latch	FD
Memory Control Latch	FC
8253 Timer Status	FB
reserved	FA
reserved	F9
reserved	F8
reserved } for manufacturing tests	F7
reserved } for manufacturing tests	F6
8041A Keyboard	F5
– 8041A Keyboard	F4
8259A Master	F3
– 8259A Master	F2
8259A Slave	F1
– 8259A Slave	F0
2661 Serial B	EF
– 2661 Serial B	EE
– 2661 Serial B	ED
– 2661 Serial B	EC

PROGRAMMING INFORMATION

Device Name	Port Address (HEX)
2661 Serial A	EB
– 2661 Serial A	EA
– 2661 Serial A	E9
– 2661 Serial A	E8
8253 Timer	E7
– 8253 Timer	E6
– 8253 Timer	E5
– 8253 Timer	E4
68A21 Parallel	E3
– 68A21 Parallel	E2
– 68A21 Parallel	E1
– 68A21 Parallel	E0

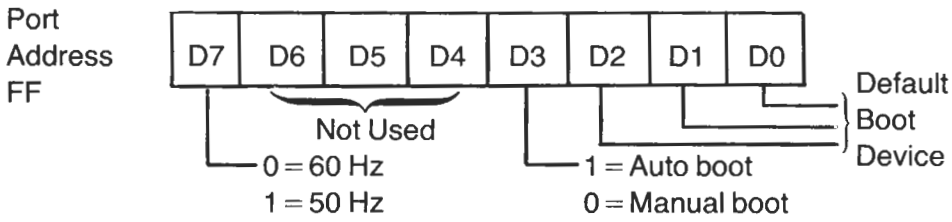
Port Bit Definitions

The definitions given below are for the bits that are written to or read from the ports listed earlier that do not connect to peripheral devices.

PROGRAMMING INFORMATION

Dip Switch Port (FF)

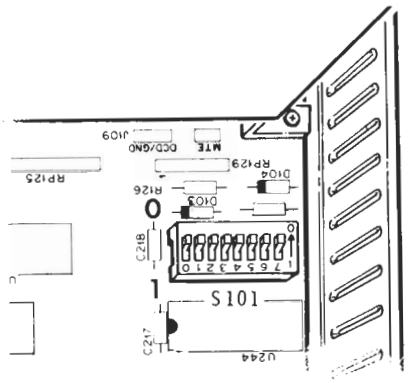
The function of the DIP switch bits are defined by the monitor program in ROM on power-up or master reset, but they may be redefined and reread by the operating system when it is loaded. The following chart gives the definition of the DIP switch's bits for the monitor ROM.



Switch S101, Section	Description
0	} Default boot device*
1	
2	
3	1 = Auto boot, 0 = Manual boot
4	not used
5	not used
6	not used
7	0 = 60 Hz, 1 = 50 Hz; for video vertical scan frequency.

*Sections 0, 1, and 2 should be set to reflect the type of drive that the system is to be booted from:

Switch Section 2	1	0	Device Type:
0	0	0	5-1/4" Floppy Disk Drive (internal)
0	0	1	8" Floppy Disk Drive (external)
0	1	0	5" Winchester Disk (internal)



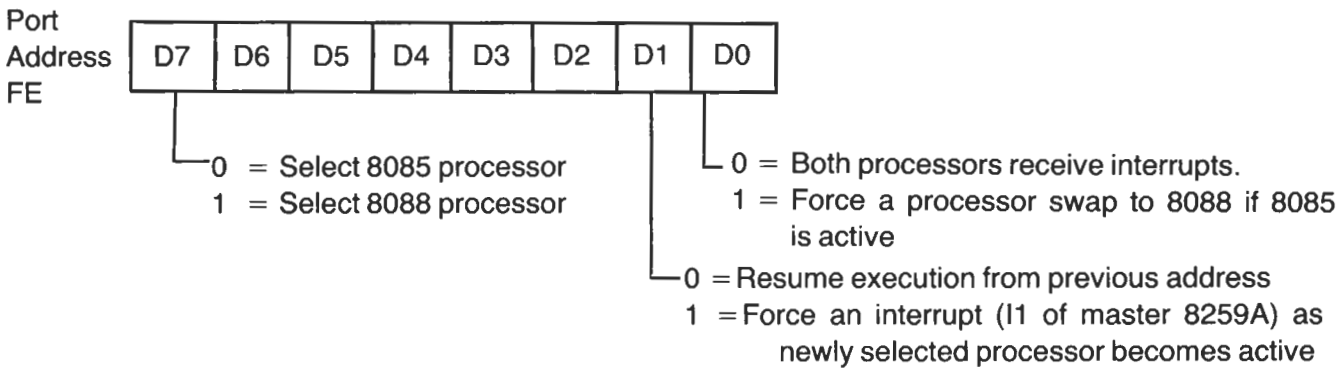
PROGRAMMING INFORMATION

Processor Swap Port (FE)

Processor swap is accomplished by the presently selected processor writing to bit 7 of the processor swap port (PSP). If a 1 is written, the 8088 is selected. A 0 selects the 8085. (See the following chart.)

When the processor swap occurs, the newly selected processor can be restarted where it left off, or, an interrupt (I1 on 8259A) can be generated. Interrupt generation is enabled by writing a 1 to bit 1 (not LSB) of the PSP.

The last option that concerns the swap port is the masking of interrupts. If interrupts are not masked, the currently selected processor is signaled when an interrupt is requested. If the MASK mode is selected, no interrupts will get through to the 8085. The 8088 will service all interrupts. In the MASK mode, a processor swap to the 8088 is generated whenever an interrupt occurs with the 8085 active. MASK is bit 0 of the PSP. A 1 activates this function.

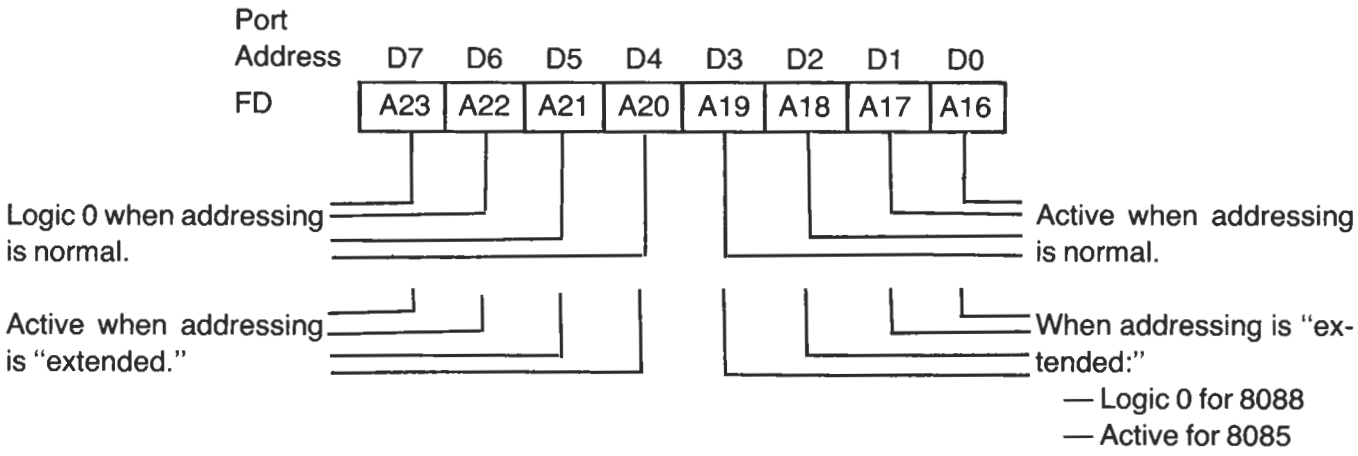


PROGRAMMING INFORMATION

High Address Latch (FD)

The 8085 in its natural state has 16 bits of addressing capability. By writing to the high address latch, HIGHADDR, the user can control the upper eight address bits placed onto the bus, and thereby generate 24-bit addresses.

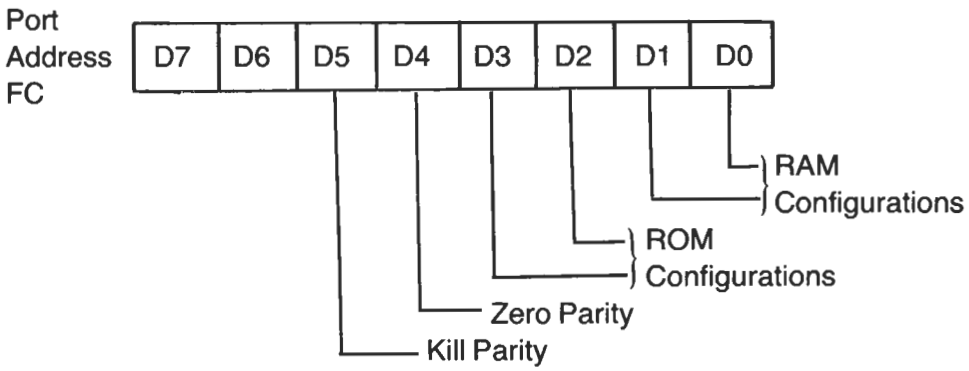
The 8088 naturally has 20 bits of addressing. The upper four bits placed on the bus are controlled by HIGHADDR. The hardware automatically selects bits A16-A19 coming from the 8088 when the 8088 is selected.



PROGRAMMING INFORMATION

Memory Control Latch Port (FC)

This port controls the configuration of memory, both ROM and RAM. It also provides an option for checking RAM parity. The options, which affect how the ROM is addressed, are enabled by writing to the memory control latch (MEMCTL) port.



The following chart shows which port bits control the various **RAM** configurations.

BITS	DEFINITION	
1,0	00 = Option 0	01 = Option 1
	10 = Option 2	11 = Option 3

Option 0, the power-up master reset configuration, provides contiguous addressing; from 0 to 192 K.

Option 1, swaps the RAM block from 0 to 48 K with the block at 64 to 112 K.

Option 2, swaps the RAM block from 0 to 48 K with the block at 128 to 172K.

Option 3, swaps the RAM block from 4 to 60 K with the block at 68 to 124 K.

PROGRAMMING INFORMATION

The following chart shows which port bits control the four **ROM** configurations.

BITS	DEFINITION	
3,2	00 = Option 0	01 = Option 1
	10 = Option 2	11 = Option 3

Option 0, the power-up or master reset configuration, makes the code in ROM appear to be in all of memory when reads are performed. Writes, however, occur normally.

Option 1 makes the ROM code appear to be at the top of every 64K page of memory.

Option 2 makes the ROM code appear to be at the top of the first megabyte of memory.

Option 3 disables the ROM.

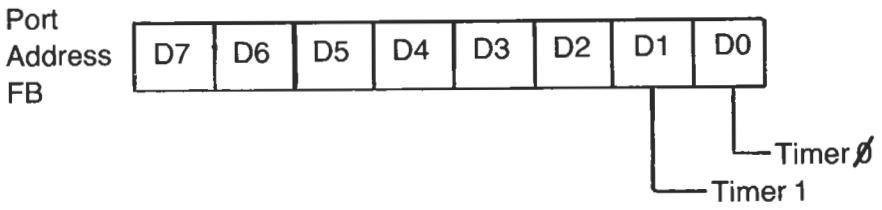
Parity consists of a parity bit for each byte in RAM. This adds one, two, or three 64K-bit chips (depending on how much RAM is installed: 64K, 128K, or 192K) and the associated support circuitry.

RAM parity has two control options: ZERO_PARITY and KILL_PARITY. The ZERO_PARITY option sets the parity to the zero state. This sets the parity bit to 0 regardless of the data pattern that was written and can be used to force a parity error to check the parity logic. The option is activated by writing a 0 to bit 4 of the Memory Control Latch (MEMCTL) port.

The KILL_PARITY option disables the parity checking circuitry by writing a 0 to bit 5 of the MEMCTL port. It also clears a parity error by first writing a 0 to bit 5 and then a 1.

PROGRAMMING INFORMATION

8253 Timer Status Port (FB)



The timer circuitry consists of an 8253 timer IC and several other IC's. (See the Timer Port Address Block Diagram.) The 8253 has three channels. Each channel has a input clock (−CLK) and an output (OUT). The CLO0 and CLK2 inputs are tied to a 250 kHz (4 μS) clock. The CLK1 input is tied to the output of channel 0, and thus channels 0 and 1 are cascaded.

Outputs OUT0 and OUT2 produce the timer interrupt input to the 8259. A latch is provided which can be read to determine which of the channels caused the interrupt (TMRSTAT). Outputs of these latches are OR'ed together to produce the interrupt input to the 8259.

To find out which timer caused an interrupt, the timer status port must be read. A high level on either the Timer 0 or Timer 1 bit indicates that the corresponding timer has had a positive transition on its OUT signal. In order to detect the next transition on the OUT signal, the latch should be cleared by writing a zero to the appropriate bit position in the timer status port.

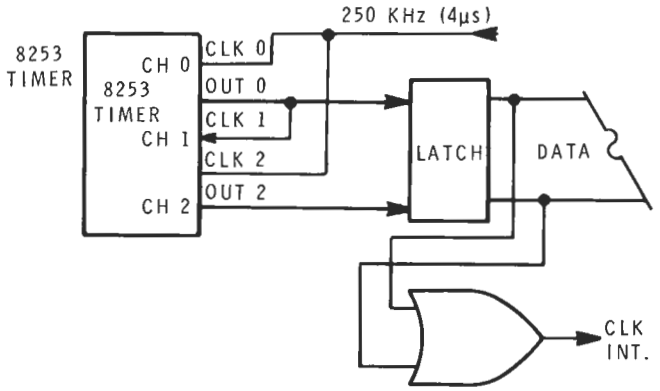
The 8253 data sheet is supplied in the Appendices portion of this documentation. The following chart is provided for the convenience of those who may already be familiar with the 8253 device.

PROGRAMMING INFORMATION

BIT	DEFINITION	
0	0 = Use 16-bit binary counter 1 = Use 4-decade binary coded decimal counter	
1 2 3	000 = Mode 0 X10 = Mode 2* 100 = Mode 4	001 = Mode 1 X11 = Mode 3 101 = Mode 5
4 5	00 = Counter latch 10 = Read/load most significant byte only	01 = Read/load least significant byte only 11 = Read/load least significant byte, then most significant byte
6 7	00 = Counter 0 10 = Counter 2	01 = Counter 1 11 = Undefined

*X = Don't care.

PROGRAMMING INFORMATION



8259A Interrupts (F0-F3)

The following list shows the possible interrupts. The slave 8259A handles only the vector interrupts you configure your hardware to generate.

Timer Port Address Block Diagram

Master 8259A

- I0 — S-100 error signal (parity error from main board memory).
- I1 — Processor swap
- I2 — Timer
- I3 — Slave 8259A
- I4 — Serial A
- I5 — Serial B
- I6 — Keyboard video display, and light pen
- I7 — Parallel printer port

Slave 8259A

I0 — VI0
I1 — VI1
I2 — VI2
I3 — VI3
I4 — VI4
I5 — VI5
I6 — VI6
I7 — VI7

} from S-100 bus

PROGRAMMING INFORMATION

68A21 Parallel Port (E0-E3)

Port Address	7	6	5	4	3	2	1	0	
E0(CRA2 = 1)	$\overline{\text{CLPHT}}$	$\overline{\text{LPSWT}}$	$\overline{\text{CVINT}}$	VIDINT	$\overline{\text{INIT}}$	STROBE	PD2	PD1	Peripheral Register A
E0(CRA2 = 0)	1	0	1	0	1	1	1	1	Data Direction Register A
E1	IRQA1	IRQA2	CA2 Control			CRA2	CA1 Control		Control Register A
E2(CRB2 = 1)	PD8	PD7	PD6	PD5	PD4	PD3	$\overline{\text{ERROR}}$	BUSY	Peripheral Register A
E2(CRB2 = 2)	1	1	1	1	1	1	0	0	Data Direction Register B
E3	IRQB1	IRQB2	CB2 Control			CRB2	CB1 Control		Control Register B

CA1 = LTPNSTB (light Pen Strobe)
CA2 = QVIDINT (Latched Vertical Sync)
CB1 = ACK (Printer Acknowledge Signal)
CB2 = BUSY (Printer Busy Signal)

The 68A21 and associated circuitry perform three functions:

- Parallel printer port
- Light pen port
- Couples video retrace signal to CPU

The 68A21 is configured as a parallel printer port. The CPU programs the 68A21 and controls it during data transfer.

PROGRAMMING INFORMATION

This printer port uses portions of both port A and port B in the 68A21. The eight bits of data out to the printer, PD1–PD8, are assigned to port A, bits 0 to 1, and to port B, bits 2 through 7 assigned to port A, bits 0 to 1, and to port B, bits 2 through 7 respectively. Data is latched at the printer by pulsing the STROBE signal (Port A, bit 2). The printer may respond by activating the BUSY signal, which can be interrogated for a level condition by reading Port B, bit 0, or for a transition by appropriate use of the CB2 input and control bits. (See the 68A21 Data Sheet in the Appendices for detailed operation.) The printer may also respond by pulsing the ACK line, which may be detected through use of the CB1 input and the CB1 control bits. The printer error signal, $\overline{\text{ERROR}}$, is read by Port B, bit 1. The printer may be initialized by activating the INIT line by Port A, bit 3.

The CPU will not respond to a signal from the light pen circuits. It requires a user-supplied program to set up interrupts, handle timing, and take care of bit locations that are pointed to by the light pen.

A pulse from the light pen is latched in a flip-flop, the output of which, LTPNSTB, is connected to the CA1 input. The flip-flop must be cleared after detecting a light pen pulse by bringing $\overline{\text{CLPHT}}$ (Port A, bit 7) low momentarily. The switch on the light pen may be read by inputting from Port A and examining bit 6, $\overline{\text{LPSWT}}$.

The vertical sync signal from the video board, VIDINT, Is also connected to the 68A21 of Port A, bit 4. The vertical sync is also latched in a flip-flop whose output, QUIDINT, is connected to teh CA2 input. By using the CA2 control bits, this input may be used to detect a transition of the vertical sync signal. This flip-flop is cleared by momentarily bringing $\overline{\text{CVINT}}$ (Port A, bit 5) low.

THEORY OF OPERATION

The Z-100 main board has five major parts: the CPU, the memory, the interrupt circuitry, the keyboard and timer, and the I/O circuitry. Each of these parts is shown in the block diagrams in Pictorials 2-1 through 2-5.

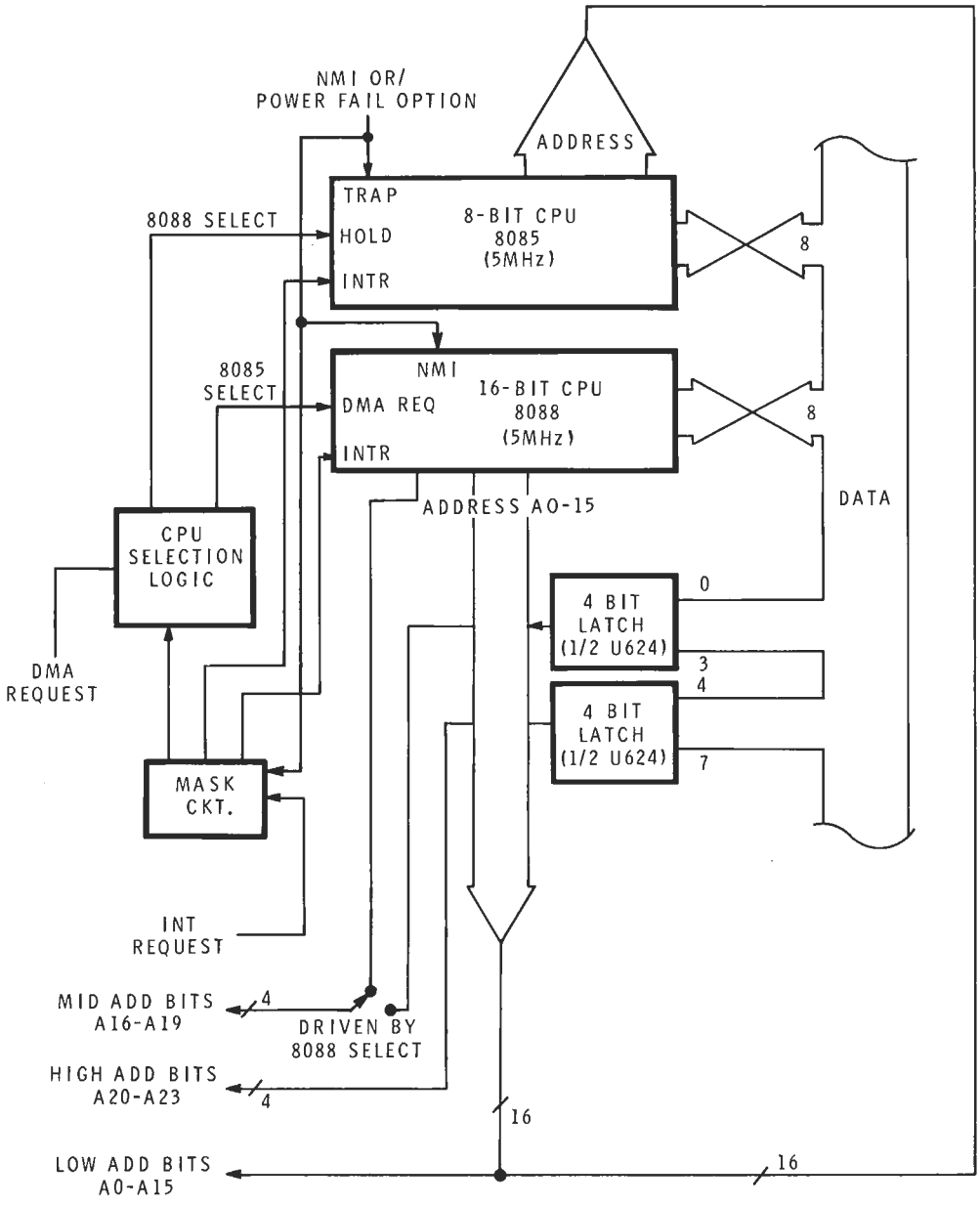
The CPU

As you can see in Pictorial 2-2, the CPU can be one of two different processors, either an 8085 or an 8088. The 8085 has 8-bit internal architecture and the 8088 has 16-bit internal architecture. They both communicate with the outside world via an 8-bit data bus.

The 8085 processor is built to generate 16-bit-wide memory addresses, but this range has been extended by 8 bits, generated through the address/data bus and latched by two 4-bit address latches. The total address width then becomes 24 bits. The 8088, on the other hand, is built to generate 20-bit addresses. This capability has been extended by 4 bits, which are similarly generated through the data bus and latched by one 4-bit address latch.

The two processors do not operate independently. Rather, they operate on an either/or basis, each being selected for use by software through the CPU selection logic. Upon power up, the 8085 is automatically selected, but the processors can be swapped at any time. When they are swapped, the newly selected processor can be restarted where it left off. Processor swapping may also occur whenever an interrupt occurs and the interrupt mask is enabled. The interrupt mask can prevent interrupts from reaching the 8085; instead, upon an interrupt, it can cause the CPU selection circuitry to select the 8088.

THEORY OF OPERATION



Pictorial 2-2
CPU Block Diagram

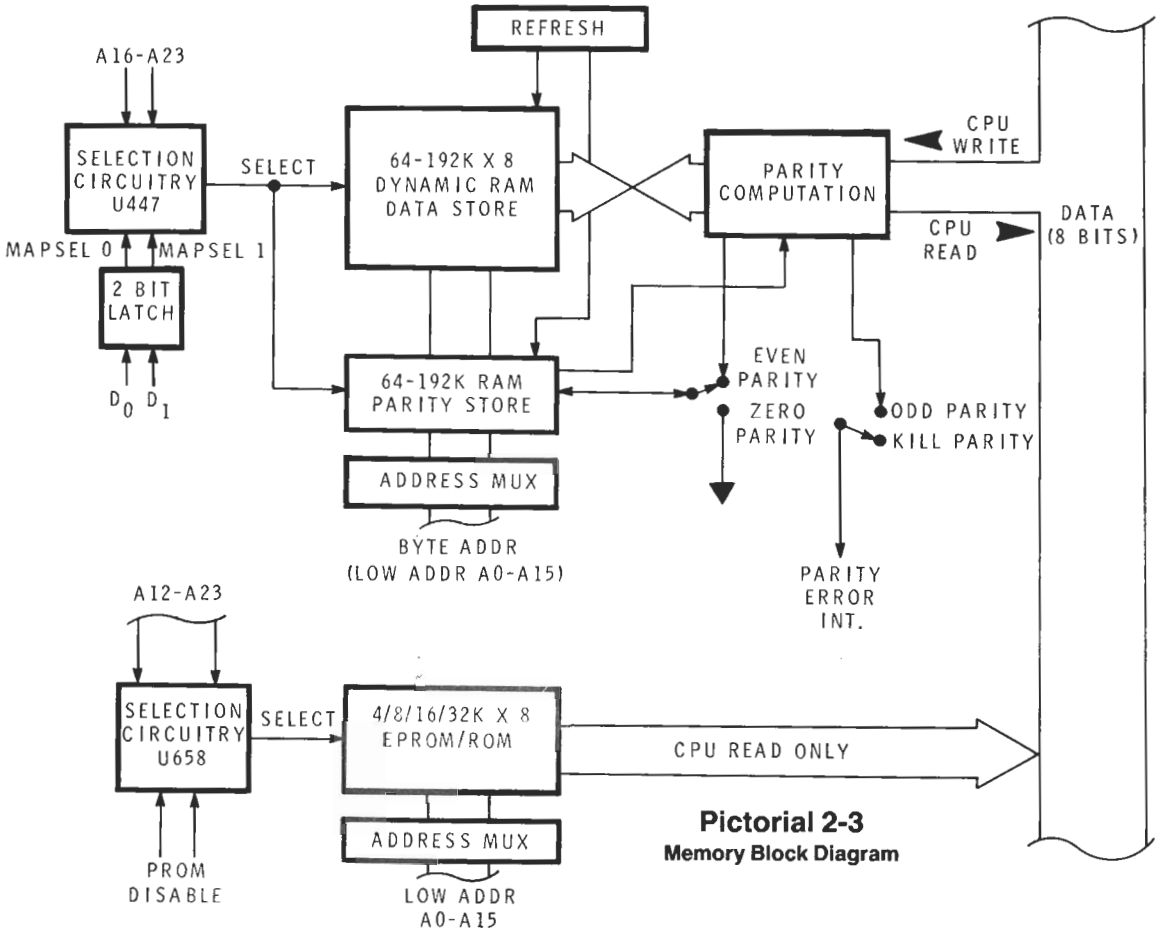
THEORY OF OPERATION

Memory

Pictorial 2-3 shows that the memory portion of the main board consists of memory selection circuitry, parity computation and storage, an address multiplexer, a refresh circuit, up to 192K of data and parity RAM, and up to 32K of ROM.

The selection circuitry decodes the address bits from the CPU to access the proper memory or port locations.

The parity computation and storage circuitry computes and stores a parity bit for every byte written into data RAM, and recomputes the parity and checks it against the value stored in parity RAM every time a word is read from data RAM. If a discrepancy is found, a parity error interrupt is sent to the 8259 interrupt controllers.



Pictorial 2-3
Memory Block Diagram

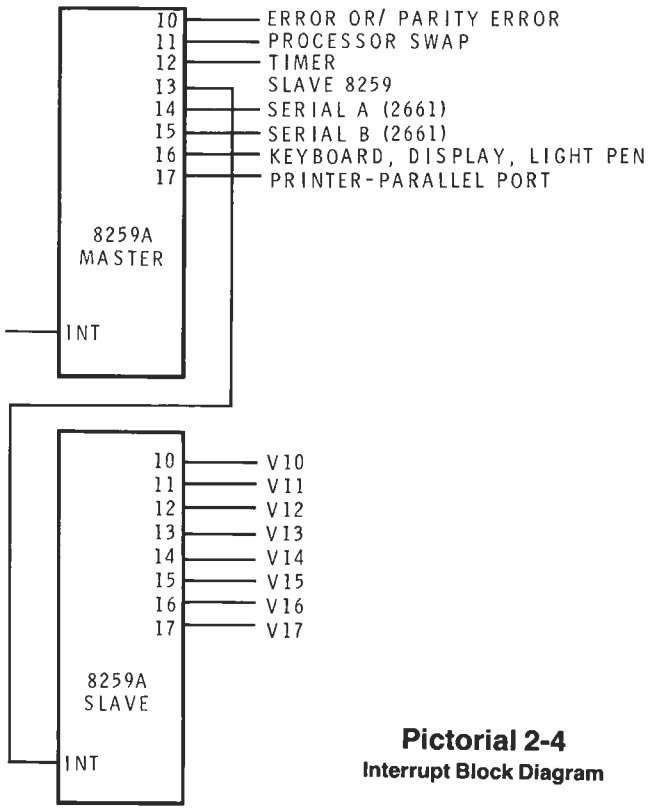
The address multiplexer converts the 16-bit address bus to the 8-bit row and column addresses required by the RAM chips.

The refresh circuit prevents the data in RAM from decaying.

The data and parity RAM is made up of 64K increments, while the ROM consists of a single EPROM or ROM chip.

Interrupt Circuitry

This circuitry consists of two 8259A interrupt processors, one a master and the other a slave. See Pictorial 2-4. The slave 8259A services vector interrupts from the S-100 bus if the hardware has been configured to use them.



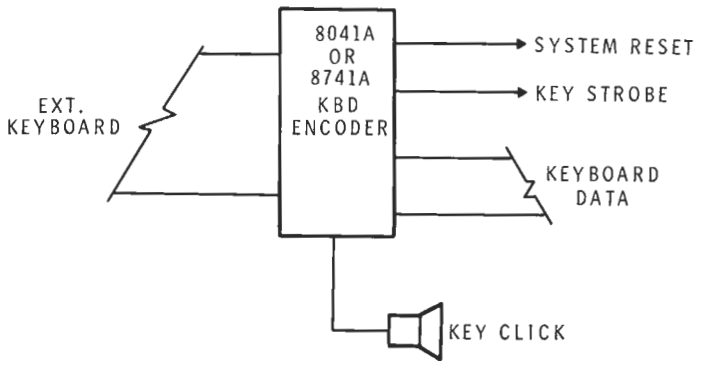
Pictorial 2-4
Interrupt Block Diagram

THEORY OF OPERATION

Keyboard

As shown in Pictorial 2-5, this circuitry is made up of a keyboard and a keyboard encoder.

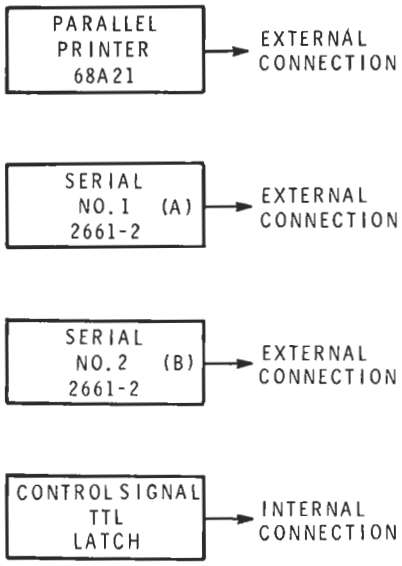
The encoder detects a closed key contact in the keyboard and converts it into the corresponding ASCII code for that key.



Pictorial 2-5
Keyboard Block Diagram

I/O Circuitry

The I/O circuitry consists of a 6821 parallel printer port, two 2661-2 serial ports, and a TTL control latch for internal use of the main board, as shown in Pictorial 2-6.



Pictorial 2-6
I/O Block Diagram

Please refer to the main board schematic while you read the following detailed description.

The 8085 CPU

General

The 8085 CPU (U210 on the schematic) is the Computer's 8-bit processor. Because the 8085 uses the same instruction set as the Intel 8080, the Z-100 computer can maintain a high degree of software compatibility with previous Zenith Data Systems Computers.

To understand the 8085, study the pin-out and basic timing discussion that follows. If you need to know more about the 8085, see the IC data sheets Appendix C of this Manual.

> **NOTE: In this and all pin-out descriptions in this Manual, active low signals may be designated as such by the traditional bar over the signal name (e.g., SIGNAL).**

Pin-Out Description

A8-A15, pins 21-28 (3-state address). These multiplexed lines contain the upper eight bits of the memory address during a memory access. During an I/O operation they contain the port address. The lines are tri-stated during HOLD, HALT, and RESET.

AD0-AD7, pins 12-19 (3-state address/data). These multiplexed lines first contain the lower eight bits of the memory address during a memory access. This address is then stored in external latches. The CPU next places the input or output data associated with that address on AD0-AD7. During an I/O operation, these lines first contain the port address, and then the data (either input or output) associated with that port.

CIRCUIT DESCRIPTION

CPU

ALE, pin 30 (address latch enable). This output line pulses high, and then low, when either the memory or I/O address is on lines A0-A7. The external circuits use the negative-going transition to latch the address information. The falling edge of ALE is also used to strobe CPU status information.

S0, S1, IO/$\overline{M}$, pins 29, 33, 34 (status output 0 & 1, input output/memory). These output lines are used in conjunction with ALE to develop the S-100 machine cycle status lines at U227. (See "Bus Status Circuits" on Page 2.35 for more details.)

$\overline{RD}$, pin 32 (3-state read control). This input line goes to logic 0 to indicate that the data bus is ready to transfer data from memory or I/O to the CPU. 3-stated during HOLD, HALT, and RESET.

$\overline{WR}$, pin 31 (3-state write control). This output line goes to logic 0 to indicate that the data bus is ready to transfer data from the CPU to memory or I/O. Data is set up on the trailing edge of the pulse. 3-stated during HOLD, HALT, and RESET.

READY, pin 35 (ready). If this input line is at logic 0, the CPU enters a wait state until READY is brought to logic 1 again. This allows using the 8085 with slow memories or peripherals.

HOLD, pin 39 (hold). If this input line is at logic 0, the CPU halts operation, raises the hold-acknowledge line (HLDA), and places the following lines into a high impedance state: Address/Data, $\overline{WR}$, $\overline{RD}$, and IO/$\overline{M}$. This allows other processors, such as the 8088, to gain control of the bus.

HLDA, pin 38 (hold acknowledge). This input line goes high to indicate that the CPU received the HOLD request and will release control of the bus in the next cycle. HLDA goes low again after the HOLD request is removed.

INTR, pin 10 (interrupt request). If this input line is brought high, and the interrupts are not disabled through software, the CPU completes its current cycle and then processes the interrupt. (See "Interrupt Circuits" for more details.)

$\overline{\text{INTA}}$, pin 11 (interrupt acknowledge). This output line goes low to indicate that the CPU has accepted the interrupt.

TRAP, pin 6 (nonmaskable interrupt). This input line is the highest priority interrupt and cannot be disabled.

$\overline{\text{RESETIN}}$, pin 36 (reset input). Bringing this input line low resets the Computer. It sets the program counter to 0, disables interrupts, and resets the HLDA flip-flop.

X1, X2, pins 1, 2 (clock input). This clock input, provided by the 10-MHz crystal at Y101, is internally divided down to 5 MHz.

CLK (clock output). This clock output provides 5-MHz timing to the Computer when the 8085 has control.

RST 5.5, pin 9. Not used and tied to ground.

RST 6.5, pin 8. Not used and tied to ground.

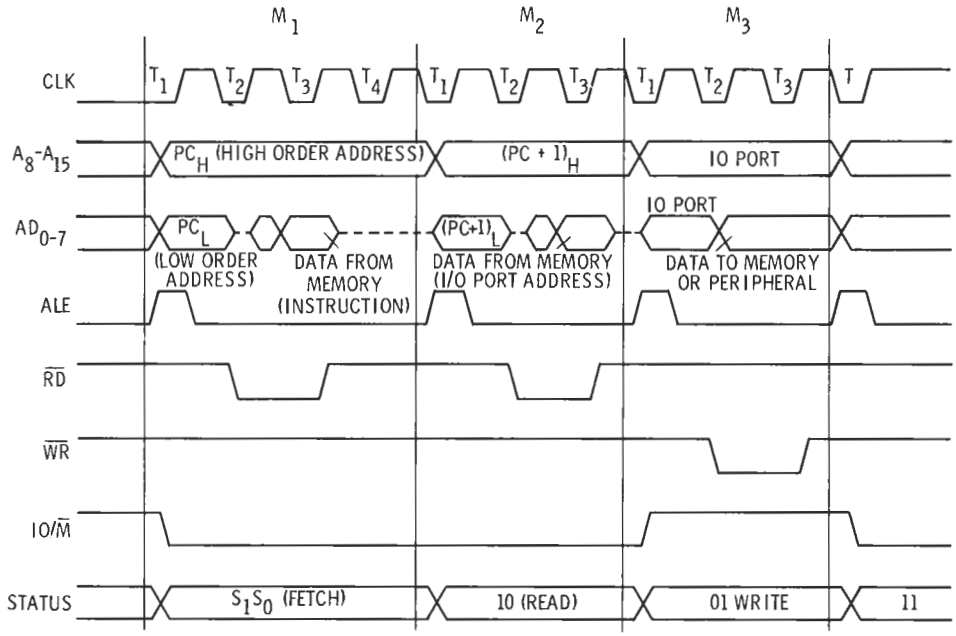
RST 7.5, pin 7. Not used and tied to ground.

SID, pin 33. Not used and tied to ground.

SOD, pin 29. Not used and left unconnected.

CIRCUIT DESCRIPTION

CPU



Pictorial 2-7
8085A Timing

Timing

To better understand how the Computer works, you should become familiar with the 8085 timing. Pictorial 2-7 shows the waveforms that occur when the 8085 processes the OUT instruction. Though there are seven possible types of machine cycles (see the data sheets), these waveforms are typical.

During the M1 cycle,the Computer fetches the op code; in this example, the OUT instruction. The M1 cycle lasts for four clock states (T-states). During this time, A8 through A15 contain the upper eight bits of the memory address of the instruction to be fetched.

From time T1 to T2, lines AD0-AD7 contain the lower eight bits of memory address. The ALE line goes low to strobe this information into the external address latches. The IO/$\overline{M}$ line goes low to indicate that this is a memory-read operation. The signals on the status lines, S0 and S1, indicate that the op code fetch cycle is taking place.

From time T2 to T3, $\overline{RD}$ goes low and the instruction in the memory location pointed to by the address latches is placed on lines AD0-AD7, which are now acting as data lines. The data, which consists of an OUT instruction, is loaded into the Computer for internal processing during time T3 to T4.

From time T3 to T4, $\overline{RD}$ goes high and AD0-AD7 goes to a high impedance state.

During the M2 cycle, the Computer reads the data in the next memory location, which is the I/O port address the Computer is to OUTput the data to. At time T1, lines A0-A15 contain the address of the memory location that holds the I/O port address. The ALE line strobes this address into the external address latches. Line IO/$\overline{M}$ is still low to indicate that the M2 cycle is a memory read cycle. This is also indicated by the logic states on status lines S1 and S0.

At time T2 to T3, $\overline{RD}$ goes low to read the memory location pointed to by the address latches. This location contains the address of the I/O port to be accessed.

During the M3 cycle, the Computer transfers the data in its accumulator to the port address specified by the M2 cycle. This time, during T1 to T2, lines AD0-AD7 contain the port address fetched during the M2 cycle. Line ALE strobes this information into the external address latches. Lines AD8-AD15 also contain the port address, but are not used. The IO/$\overline{M}$ line goes high to indicate that this cycle is an I/O cycle, rather than a memory cycle. Also, the logic states of the status lines, S0 and S1, indicate that this cycle is an I/O write cycle.

During time T2 to T3, the data in the accumulator of the 8085 is placed on the data bus and $\overline{WR}$ goes low to write it to the port pointed to by the address latches.

After T3, the 8085 generates another M1 cycle and fetches the next instruction in the program.

CIRCUIT DESCRIPTION

CPU

The 8088 CPU

General

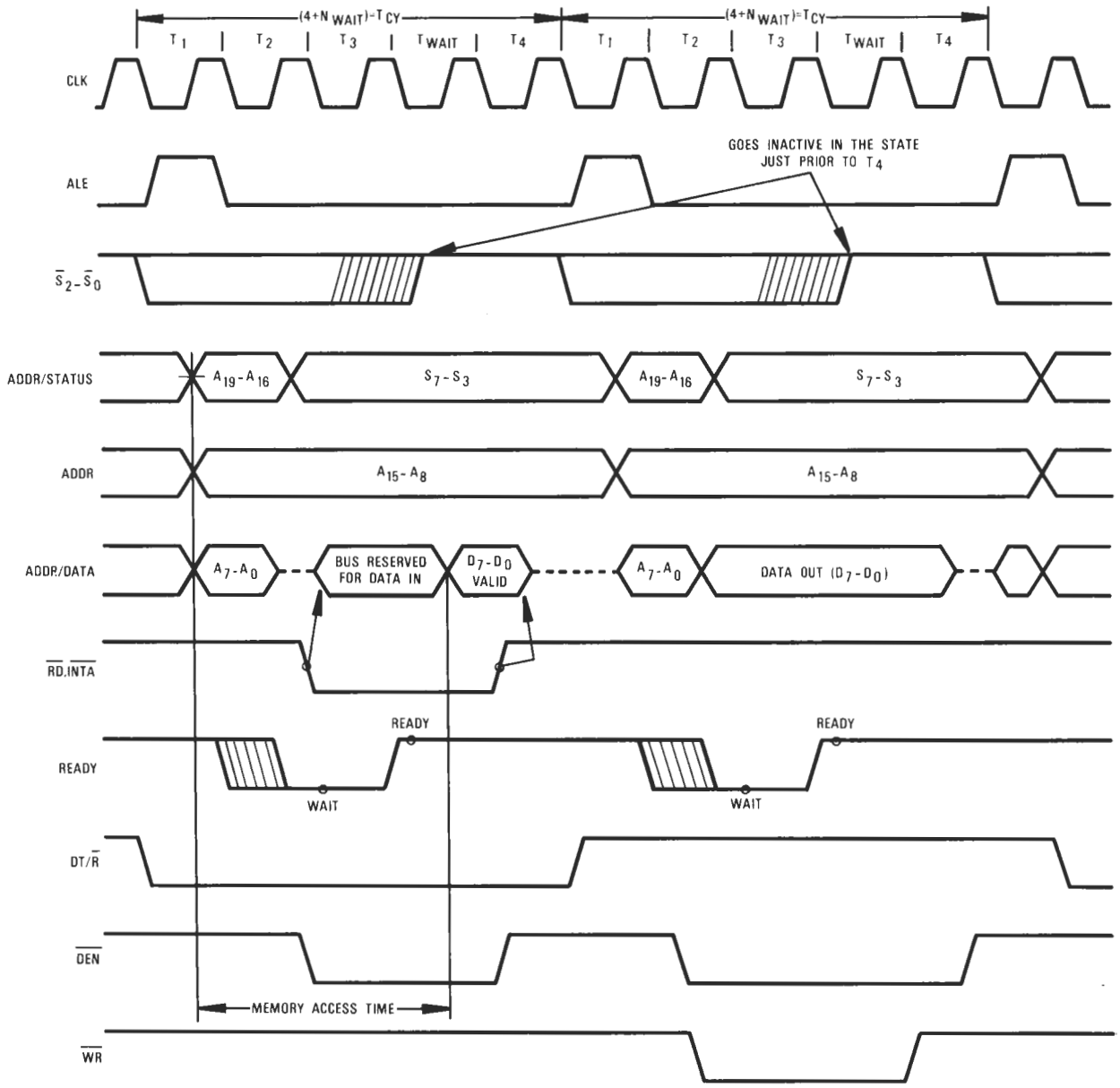
The 8088 CPU is the Comupter's 16-bit processor, which is located at U211 on the schematic. This IC combines the resources of a 16-bit microprocessor's internal architecture with the easy-to-use 8-bit bus interface. In fact, most of the functions of the bus lines in the 8088 are identical to the 8085 at U210.

Some of the features of the 8088 are:

- A 20-bit address bus, allowing the 8088 to directly address up to 1 megabyte of memory.
- A 16-bit input/output port address range, allowing the 8088 to select up to 65536 port addresses. However, only the lower eight bits are used in Z-100 Series Computers.
- Pipelined architecture to allow fetching instructions and processing previously-fetched instructions at the same time. (Refer to the "iAPX 88 Book" in Appendix C.)

Pin-Out Description

Refer to Pictorial 2-8 while you read the following paragraphs.



Pictorial 2-8
8088 Timing

CIRCUIT DESCRIPTION

CPU

$\overline{RD}$, pin 32 (read strobe). This line goes low when the CPU reads from memory or an I/O port, and goes to a high impedance state during hold acknowledge (HLDA).

$\overline{WR}$, pin 29 (write strobe). This line goes low when the CPU writes to memory or an I/O port, and goes to a high impedance state during HLDA.

IO/$\overline{M}$, pin 28 (status line). This line goes low during a memory read or write ($\overline{RD}$ or $\overline{WR}$ asserted). It is logic 1 for an I/O read or write. It is 3-stated during HLDA.

DT/$\overline{R}$, pin 27 (data transmit/receive). This line is similar to IO/$\overline{M}$.

$\overline{SSO}$, pin 34 (status line). This line is used with DT/$\overline{R}$ and IO/$\overline{M}$ to develop the S-100 status circuit signals. The logic levels on this line depend on what type of instruction the CPU is processing. This line is brought to a high impedance state during HLDA.

ALE, pin 25 (address latch enable). This line pulses high when the CPU places the address information on the address/data bus. In the Computer, this line clocks the address into external latches on the negative-going edge of ALE.

AD0-AD7, pins 16-9 (address/data bus). When ALE is asserted, these lines contain the lower eight bits of the 20-bit address. This can be a memory address or an I/O port address. Later in the machine cycle, when data is to be transferred, these lines contain the input or output data. Demultiplexing circuits in the Computer are used to separate the data and address information. These lines are 3-stated during HLDA.

A8-A15, pins 2-8 & 39 (address bus). These lines carry the next eight bits of the address. This is memory address during a memory access and I/O address during the port access. These lines hold the address during the entire bus cycle. They are 3-stated during HLDA.

NMI, pin 17 (non-maskable interrupt). A positive-going transition on this line interrupts the CPU. It cannot be blocked with software. The CPU will complete its current instruction and then service the interrupt.

INTR, pin 18 (interrupt request). The CPU tests this line during the last clock cycle of each instruction to see if some device is requesting an interrupt. If pin 18 is logic 1, then an interrupt request is taking place. The CPU processes the interrupt unless the interrupt is masked by software.

$\overline{\text{INTA}}$, pin 24 (interrupt acknowledge). The CPU brings this line to logic 0 to inform the interrupting device that it is processing the interrupt. It is used as a read strobe to get vector information from the interrupt circuits (see the interrupt circuit description for more details).

HLDA, pin 30 (hold acknowledge). This pin goes high to indicate that the CPU has acknowledged a hold request at pin 31.

HOLD, pin 31 (hold request). This line goes high when another device requests control of the bus, such as when the 8085 is the active processor. The CPU asserts the HLDA line and suspends operation.

A19-A16, pins 35-38 (address/status bus). These lines hold the top four bits of the 20-bit address bus when the ALE is active. ALE clocks this value into external latches when it returns to 0. These lines contain status information during the last part of the machine cycle. This feature is not used in the Computer since it gets the status information in a different manner. These lines are 3-stated during HLDA.

$\overline{\text{TEST}}$, pin 23 (test input). This input is examined by the "WAIT FOR TEST" software instruction. If pin 23 is low, execution continues. Otherwise, the processor waits in an idle state.

CIRCUIT DESCRIPTION

CPU

MN/$\overline{MX}$, pin 33 (minimum/maximum). A logic 1 on this pin places the 8088 in the minimum mode, the mode used by the Computer. When it is placed in the maximum mode, some of the pin functions change. Usually, the maximum mode is used for larger systems and multiprocessing systems.

RESET, pin 21 (reset). This pin goes high to reset the 8088. The interrupts are disabled, certain registers in the 8088 are set or cleared, and the instruction pointer (program counter) points to the address 16 bytes below the top end of the 1 megabyte range (FFFF0H).

The line is asserted when the $\overline{RESET}$ line at U236, pin 11 is pulled low. A Schmitt trigger shapes up this signal and the clock retimes it before applying it to the 8088.

READY, pin 22 (ready). This is an acknowledgement signal from the addressed memory or I/O port that it is ready to transfer data. When this line is low, the CPU goes into a wait state until the addressed device brings it high. This allows using the 8088 with slow memory or I/O devices.

The READY signal is generated when U205-9 places a logic 1 on U236, pin 4. U236 synchronizes this signal with the 8088 clock to ensure correct set-up and hold times.

CLK, pin 19 (8088 clock input). This is a 5-MHz clock that provides timing to the 8088.

This signal comes from U236, pin 8, which derives it from the 15-MHz crystal at Y103. Duty cycle is about 33% for optimized timing inside the 8088. [When the 8088 is the active processor, this line (88Φ) also goes to the CPU dock swap logic to provide system timing.]

Timing

Timing for the 8088 is essentially the same as the timing for the 8085, since the 8088 is operated in the "min" mode.

Processor Swap Port

General

The processor swap port controls which CPU is to be active, handles interrupt routing, and ensures proper timing of the clock circuits during the swap. To access the swap port, the CPU writes a control byte to port 0FEH. Only three bits of the byte are used: AD0 controls the automatic wrap and/or mask mode, AD1 controls the swap interrupt line, and AD7 performs the processor swap.

At power up, the reset circuits clear U171 pin 9 to logic 0. This pin, 8SEL, connects to U186, a 12H6 PAL, through pin 5. This IC responds by placing a logic 0 on U187 pin 12 and a logic 1 on U187 pin 2. On the first positive transition of $\overline{85\Phi}$, the 85HOLD line goes low, enabling the 8085 CPU. On the first positive transition of $\overline{88\Phi}$, the 88HOLD line goes high, disabling the 8088 CPU.

The 8085, while executing the code in the monitor ROM, soon transfers control to the 8088. It does this by setting bit 7 of the processor swap port control byte to logic 1 by writing to that port.

The CPU address port 0FEH asserts $\overline{\text{SWAPCS}}$ (from the I/O decoder) at U206 pin 5. It then sets AD7 to logic 1 at U171 pin 12. Finally, it asserts the write line at U206 pin 6. As a result, U171 pin 11 goes high and latches U171 pin 9 to logic 1. The 8SEL line is now asserted. The values at U172 pin 12 and U172 pin 2 are also latched to their respective outputs.

The 8SEL line, now logic 1, causes U186 pin 13 to change to logic 1, pin 18 to change to logic 0, and pin 16 to change to logic 1. This last line, 88SEL, couples to U215 to form the S-100 bus line (pin 21), NDEF (8088). This line is a "not-to-be-defined" line that can be used for any function. In the Computer, this line asserts when the 8088 is active.

CIRCUIT DESCRIPTION

CPU

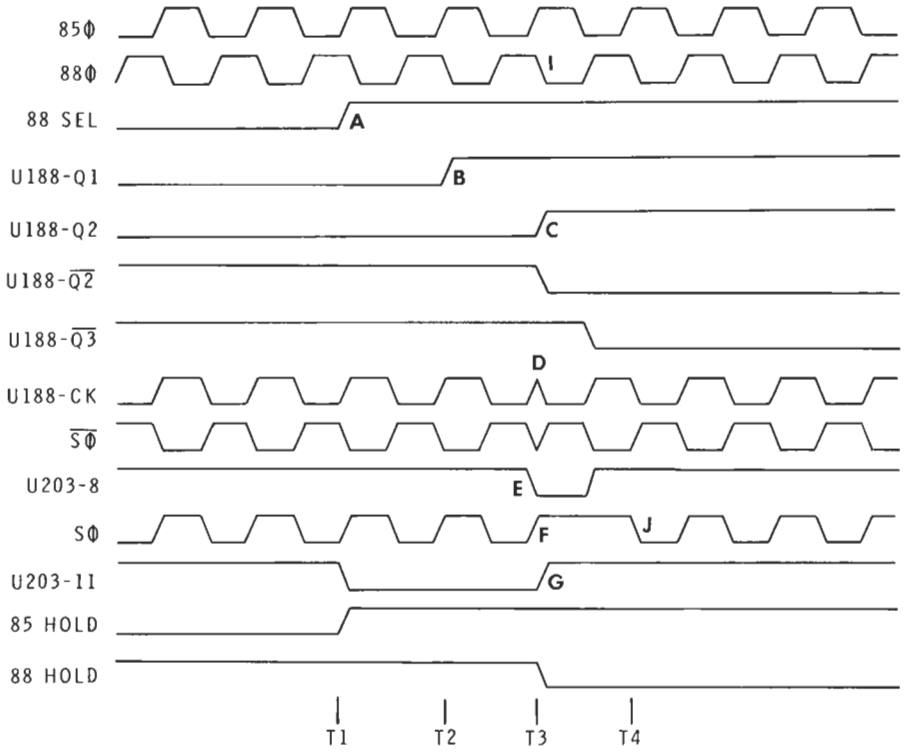
The HOLD* line at U185 pin 11 asserts whenever a board on the S-100 bus takes control of the Computer. This causes U186 to disable both the 8085 and the 8088 through U187. Both CPUs respond by returning their HLDA signals; the 8088 at U186 pin 3 and the 8085 at U171 pin 2. When this happens, U188 asserts the HAK line at pin 17. This, in turn, raises the S-100 pHLDA line to logic 1 at U180 pin 9. The board that generated the HOLD* request can now take control of the Computer.

Swap Timing

The 88SEL line also goes to U188, pin 4, a quad D-type latch that suppresses any glitches on the system clock line when the Computer switches from one CPU to the other. It also ensures that the CPU being disabled is no longer active when the other CPU is enabled.

The 8085 and the 8088 run on separate crystal-controlled clocks; the 8085 from Y101 and the 8088 from Y105. Although these clocks are stable, they are not in phase. Switching from one clock to another can cause a glitch on the system clock line, SΦ, that can upset the timing in other circuits.

To see how U188 and its associated circuits block this spike, refer to Pictorial 2-9.



Pictorial 2-9
Switching from 8085 to 8088

The two top waveforms are the respective clocks for the 8085 and 8088 CPUs. These are present at the inputs of inverters U200 pin 2 and U200 pin 14. Assuming that the 8085 is the active processor, then U200 pin 1 is low and $\overline{85\Phi}$ couples through the inverter to form $\overline{S\Phi}$. It also couples through U225B to clock U188.

At time T1, the 8088 is selected; the 88SEL line goes to logic 1 as shown at A in Pictorial 2-9 (waveforms illustration). On the next positive edge of the clock at U188 pin 9, this logic 1 latches into U188 pin 2, which is the Q1 output at B. The next clock pulse causes the Q2 output to latch high, shown at C.

CIRCUIT DESCRIPTION

CPU

When Q2 goes high, it 3-states U200 through the exclusive-OR gate at U203B. At the same time, $\overline{Q2}$ goes low to couple the 88Φ clock to the $\overline{S\Phi}$ line. Since, in this example, the two clocks are nearly 180 degrees out of phase, the clock immediately returns to 0, causing the spike at D in Pictorial 2-9.

Up until this time, the output of U203, pin 8, another exclusive-OR gate, has been logic 1. This is because its inputs Q2 and $\overline{Q3}$ of U188 have been in opposite states. However, since Q2 went high at time T3, both inputs to U203C are the same, causing U203 pin 8 to go to logic 0 (waveform E). This forces the system clock output at U225 pin 3 to logic 1 until time T4 (waveform F).

At time T4, the first positive-going edge of the 8088 clock causes the $\overline{Q3}$ output of U188 to go high. This opens the gate at U225A to pass the system clock, which is now the 8088 signal.

As mentioned earlier, the other function that 88SEL and U188 performs is to ensure that the CPU being disabled is completely disabled before the CPU to be enabled is activated. To see how this is done, again refer to Pictorial 2-9.

Assume as before that the Computer is switching from the 8085 to the 8088. At time T1, the 88SEL line, which is coupled to U203 pin 11, goes high, the other input of this exclusive-OR gate is the $\overline{Q2}$ U188. Since both inputs are now the same state, U203, pin 11 goes to logic 0 to preset both HOLD latches at U187.

Both CPUs go into a HOLD state and keep HLDA signals asserted at U186; the 8088 to pin 3 and the 8085 to pin 4 through U171.

At time T3, the $\overline{Q2}$ line goes low and U203 pin 11 returns to logic 1, releasing the latches at U187 from their preset states. On the next positive-going edge of the $\overline{88\Phi}$ clock signal, the logic 0 at U187 pin 2 is latched into U187 pin 5, removing the 8088 from the hold state.

U188 pin 7 goes high to drive U215 pin 3 high. This last IC connects to pin 21 of the S-100 bus to form the NDEF (8088/$\overline{8085}$) line. This line is a "not-to-be-defined" line that can be used for any function by the computer manufacturer. For the H/Z-100 Series Computer, this line asserts when the 8088 is active.

The same process takes place when control of the system is switched from the 8088 to the 8085; the only difference is that the Q outputs of U188 are going from logic 1 to logic 0. (See the bottom group of waveforms in Pictorial 2-9.)

Auto Swap On Interrupt/Mask Mode

The interrupt mask circuits ensure that interrupt requests are sent to the currently active CPU. The mask bit, MSK, is set or cleared by setting or clearing bit 0 of the processor swap port. If cleared, and the 8085 is active, the 8085 gets all interrupt requests. If set, and the 8085 is active, the interrupt request is blocked but the swap port disables the 8085 and enables the 8088. If the 8088 is active, all interrupt requests are sent to the 8088 regardless of the mask bit.

After reset, 5SEL at U171 pin 8 and $\overline{MSK}$ at U172 pin 6 are logic 1, so that the 8085 is active and handles all interrupts. These two lines connect to U225 pin 9 and U225 pin 10, which are shown near the 8085 on the schematic. U220 pin 2 inverts the resulting logic 0. This enables U189A and U189D. U189D can now couple non-maskable interrupts to the trap input of U210, and U189A can pass standard interrupts to U210's interrupt request input.

The 8SEL line, which is the complement of 5SEL, disables U189B and U189C, the AND gates to the 8088.

If, while the 8085 is selected, the $\overline{\text{MSK}}$ line is set to logic 0, then U220 pin 2 disables U189A and U189D. This blocks the interrupt request from both the 8085 and the 8088. However, if either a standard or an NMI interrupt request occurs, U156 pin 6 will go high to assert the NMINT line.

This line connects to U155 pin 9 in the processor swap port. The other input is the MSK line which is also high. As a result, U155 pin 8 goes low to assert the 8SEL line. The Computer switches to the 8088 processor as described previously.

When the 8088 is active, 8SEL is high to enable U189B and U189C. U189A and U189D are disabled because 5SEL is logic 0 at U225 pin 9. So, no matter what the setting of the $\overline{\text{MSK}}$ bit at U225 pin 10, all interrupt requests are routed to the 8088 processor.

Swap Interrupt

Whenever one of the CPUs is placed into the HOLD state, it does not lose the contents of its registers. This way, when that CPU is again enabled, it can begin processing where it left off.

Alternatively, the currently active CPU can generate a swap interrupt to start the disabled CPU at a different memory location than where it was when it was turned off. It does this by programming the master 8259A to mask all interrupts except the swap interrupt, and then it asserts the SWAPINT line.

To generate the swap interrupt command, the Computer sets bit 1 to logic 1 in the processor swap port. It does this by asserting $\overline{\text{SWAPCS}}$ (from the I/O decoder) at U206 pin 5, setting AD1 to logic 1 at U172 pin 12, and then asserting the $\overline{\text{WR}}$ line at U206 pin 6. U206 pin 4 goes high to latch U172 pin 9 to logic 1, sending the SWAPINT command to the interrupt circuits.

At the same time, the CPU also writes the correct control bits to 8SEL and MSK on the processor swap port. The Computer changes CPUs, finds that the SWAPINT line is asserted, and jumps to the correct location to process the interrupt.

Reset Circuits

Power-Up Reset

R114 and C189 provide the power-up reset signal for the Computer. Upon turn-on, C189 charges through R114, holding U207 pin 8 low for about 200 ms. This signal connects to several buffers to provide the proper reset levels to the rest of the computer:

U201B buffers the reset signal to provide the S-100 power-on clear (POC*) signal. This signal is logic 0 for reset and logic 1 otherwise. POC* resets the video board through U215D and P106 pin 64.

U201A buffers the reset signal to provide the S-100 SLAVE CLR* signal. Because U207 pin 8 controls U201A through its gate line (pin 1), SLAVE CLR* is logic 0 to clear and open-collector otherwise. This signal is present only to meet IEEE-696 (S-100) standards. Currently, it is not used in the Computer.

U210C is also wired to provide a logic 0 for reset and a high-impedance state otherwise. This is because several circuits may share the S-100 RESET* line. This line drives U177H and, through the S-100 bus, resets the Floppy Disk Controller Board.

U177H inverts the reset signal, which can be the power up reset or a keyboard reset, to drive the RESET line high. This line is again inverted by U177G and U177F to provide $\overline{\text{RESET1}}$ and $\overline{\text{RESET2}}$; all three lines go to several places on the motherboard and video board to provide the proper reset signals.

CIRCUIT DESCRIPTION

Keyboard Reset

When you press the CRTL key and the RESET key at the same time, pins 8 and 9 of U103 go low and force U183 pin 10 to logic 1. This is inverted at U183 pin 4 and coupled to U185A through the filter network, R109 and C174.

U185B and U185C invert the signal twice to provide the active-low $\overline{\text{KBDRESET}}$ pulse that couples to U201 pin 13. The output, U201 pin 11, is logic 0 for reset and high-impedance otherwise.

From U201 pin 11, the reset signal is processed as described earlier in "Power-Up Reset."

Dip-Switch Select Circuits

U239, S101, and U156A make up the DIP-switch select circuits. The position of these switches determine the operating mode of the Computer.

The Computer reads the status of S101 during power-up by addressing input port 0FFH. To read the DIP-switch port, the CPU asserts the $\overline{\text{DSWSEL}}$ port select line coming from the I/O port decoder at U159 pin 7. The CPU also asserts the S-100 pDBIN line to indicate that an I/O read operation is to take place. U195 inverts the pDBIN line to produce $\overline{\text{DBIN}}$ at U156 pin 2.

Since pins 1 and 2 of U156 are both low, pin 3 of this OR gate also goes low to enable U239. The outputs of U239 go from a high-impedance state to the logic level of each switch section. This, in turn, is loaded into the accumulator of the CPU for further processing.

S-100 Bus Status Circuits

The IEEE-696 S-100 bus contains eight status lines, because there are eight basic types of machine cycles. The Computer uses all but one of these lines. The unused line, sXTRQ*, is still available for use by plug-in boards.

Following the S-100 (proposed IEEE-696) standard, the status lines designations are prefixed with a lower-case "s." All but two of the lines, sWO* and sXTRQ*, assert on logic 1. Briefly, this is what each status line does:

sXTRQ*, pin 58 (sixteen-bit request). This line allows 8-bit and 16-bit boards to share the same bus. Since the Computer is an 8-bit machine externally and a 16-bit machine only inside the 8088, this line is kept disabled by connecting U227 pin 18, to logic 1.

However, if a true 16-bit CPU board is plugged into the S-100 bus, the Computer can be programmed to give control to this CPU, and this CPU can perform 16-bit transfers with other 16-bit boards on the bus.

It does this by asserting sXTRQ* and addressing the 16-bit board (U227 pin 19 is 3-stated at this time by a low at U182 pin 9). If the addressed device can process 16-bit words, it asserts another S-100 line called SIXTN*. Next, the data buses are ganged together; lines DO0-DO7 handle even bytes while lines DI0-DI7 handle odd bytes, and the data transfer takes place. (Odd bytes is defined as A0 = 1, and even bytes as A0 = 0.

If the device cannot process 16-bit words, such as memory and I/O on the motherboard and video board, SIXTN* remains high. In this case, DO and DI lines operate normally and the CPU must process the data a byte at a time.

CIRCUIT DESCRIPTION

CPU

sM1, pin 44 (op code fetch). This line asserts when the 8085 processor fetches a new instruction from program memory. It returns to logic 0 at the end of the M1 machine cycle. However, when the 8088 is operating, the asserted sM1 line does not guarantee the fetch of a new instruction. It only indicates that a "code access" has been decoded by the 8088. (In future versions of the Z-100 Computers, the 8088 might not assert the sM1 line at all.)

sOUT, pin 45 (write to output port). This line asserts to indicate that the CPU is going to send data to the addressed output port.

sINP, pin 46 (read from input port). This line asserts to indicate that the CPU is going to read data from the addressed input port.

sMEMR, pin 47 (memory read). This line asserts to indicate that the CPU is going to read data from the addressed memory location.

sHLTA, pin 48 (halt acknowledge). This line asserts when the CPU processes a HALT command and has stopped executing the program.

sINTA, pin 96 (interrupt acknowledge). This line asserts when it is processing an interrupt.

sWO*, pin 97 (memory write). This line asserts when the CPU is going to write data to either memory or an output port.

These lines are derived from the status lines of whichever CPU is active. In the 8088, these lines are IO/$\overline{M}$, DT/$\overline{R}$, and $\overline{SSO}$. In the 8085, these lines are IO/$\overline{M}$, S1, and S0.

When the 8088 is active, the 88SEL line at U226 pin 13 is logic 1. This causes the 32 × 8 PROM to correctly decode the bit pattern on pins 10, 11, and 12 as an 8088 status code. As you will see later, this code is different for the 8085.

88SEL also 3-states 85S0 and 85S1 at pins 1 and 4 of U237. The line from 85IO/$\overline{M}$ is in a high-impedance state when the 8085 is disabled, so it does not need a buffer.

U226 decodes the machine cycle status and asserts the correct line on the output. U226 pin 1, through U226 pin 7. When the ALE line goes low, the outputs of U226 are latched into U227.

When the 8085 is active, the 88SEL line at U226 pin 13 is logic 0. This causes U227 to correctly decode the bit pattern on pins 10, 11, and 12 as an 8085 status code. U226 decodes this status which is subsequently latched into U227 when ALE goes low.

The following chart shows the status codes of each CPU and what S-100 status line each code affects.

8085				8088				S-100
IO/$\overline{M}$	S1	S0	Status	IO/$\overline{M}$	DT/$\overline{R}$	$\overline{SS0}$	Status	Status
0	1	1	Op code fetch	0	0	0	Code access	sM1, SMEMR
1	0	1	I/O write	1	1	0	Write I/O port	sOUT, SW0*
1	1	0	I/O read	1	0	1	Read I/O port	sINP
0	1	0	Memory read	0	0	1	Memory read	sMEMR
Z	0	0	HALT	1	1	1	HALT	sHLTA
1	1	1	Interrupt Ack.	1	0	0	Interrupt Ack.	sINTA
0	0	1	Memory write	0	1	0	Write memory	sWO*

Z = High impedance at CPU IO/$\overline{M}$ 3-state line.

CIRCUIT DESCRIPTION

CPU

Wait Timing

The WAIT line at pin 9 of U226 equalizes the timing characteristics between the 8085 and the 8088. It does this by adding the appropriate wait states during a memory or I/O access. The number of wait states depends on the active CPU and the type access, as shown in the chart below.

	Wait Timing	
	8085 Active	8088 Active
Memory Access	1 wait state	0 wait state
I/O Access	2 wait states	1 wait state

U233 pin 5 provides the basic wait timing. When ALE asserts, pin 5 is cleared. After ALE goes low, pin 5 goes high on the next system clock pulse. If the machine cycle is a memory or I/O access, the wait line asserts according to the chart above.

The asserted wait line is inverted by U206A to clear pin 9 of U205. This logic 0 couples directly to the 8085 READY input and indirectly to the 8088 READY input through U236. The active CPU goes into a wait state until the next system clock pulse at pin 11 of U205. Operation then proceeds normally.

The RDY and XRDY lines are S-100 "ready" lines. If either line is low, the CPU goes into a wait state at the end of a machine cycle, as follows.

The ALE line clears U205 at the beginning of each machine cycle. Both RDY and XRDY are normally logic 1 at pin 12 of U205. Unless the wait line is asserted, the next clock pulse will latch U205 pin 9 to a logic 1, ensuring that the active CPU will not generate a wait state during that machine cycle.

If either RDY or XRDY should go low, U205 pin 9 remains at logic 0 during that bus cycle. This causes the CPU to go into a wait state at the end of the cycle. (See the 8085 and 8088 data sheets in Appendix C for the exact timing relationships.) To see how the Computer uses the RDY line, refer to the "Video Board" (Page 4-56) "Disk Controller" (Page 6-29), and the "Memory" (Page 2-50) sections in this Manual.

S-100 Bus Control Output Circuits

The five lines of the bus control output circuits determine the timing and movement of data during any bus cycle. The mnemonics of these lines always begin with a lower-case "p." Refer to the 8088 timing waveforms in Pictorial 2-8 as each output line is discussed.

pSYNC, pin 76 (synchronization). This line goes high to indicate the start of a new bus cycle. Basically, it is the ALE signal of the currently active CPU retimed to the rising edge of the system clock.

In the 8088, the ALE line goes high at the beginning of the bus cycle. This couples through U221A to latch a logic 1 on U219 pin 5. Halfway through state T1, the system clock goes high at U219 pin 11. This causes U180 pin 3 (the pSYNC output) to go high. At the same time that pSYNC asserts, U219 pin 8 goes low to clear U219A at pin 1.

During state T2, the next positive-going edge of the system clock latches U219 pin 9 to logic 0; the pSYNC line is no longer asserted and U219A is no longer held cleared.

pSTVAL*, pin 25 (status valid). The line works in conjunction with pSYNC to indicate when the S-100 address and status lines are valid.

CIRCUIT DESCRIPTION

CPU

Inverted pSYNC couples from U219 pin 8 to U234 pin 12, and inverted system clock connects to U234 pin 11. Between state T1 and T2, the inverted pSYNC is logic 0. The rising edge of $\overline{S\Phi}$ latches this onto U234 pin 9, which is buffered through U180B to form the pSTVAL* signal.

On the next rising edge of $\overline{S\Phi}$ between T2 and T3, the inverted pSYNC has returned to logic 1. This is coupled through U234B and U180B to the pSTVAL* line.

pDBIN, pin 78 (data bus in). This is a generalized read strobe that gates data from memory or an input port to the data bus.

The pDBIN signal is derived by NORing $\overline{CPURD}$ and pSYNC at U206C. This ensures that pDBIN will not assert until after the negative-going edge of pSYNC, which occurs after the negative-going edge of pSTVAL*.

pHLDA, pin 26 (hold acknowledge). This is the hold acknowledge signal; it goes high when both the 8088 and the 8085 are in a hold state. Such a situation can occur if a board plugged into the S-100 bus must take control of the bus, such as when a DMA transfer is to take place.

The device requesting control of the bus asserts the S-100 HOLD* line at U185 pin 11. U186 pin 8 detects this logic 1 and writes logic 1 to U187 pins 9 and 5. These lines send HOLD commands to the 8085 and 8088.

In our example, the 8085 is already in a hold state, so the 85HOLD line is already high. However, the 8088 is active. When it detects the asserted 88HOLD line, it finishes the current instruction and indicates a hold acknowledge status by asserting 88HLDA at U186, pin 3.

Pin 4 of U186, the 85HLDA, is already asserted, so U186 pin 17 goes high. This line, HAK, couples through U180D to form pHLDA.

pWR*, pin 77 (valid write data). This is a generalized write strobe that writes data from the data bus into memory or an output port. It is timed with pSYNC and pSTVAL* to ensure that the data is valid on the D0 bus before a write takes place.

The CPU write command is inverted through U220 pin 12 and applied to U235 pin 13, a three-input NAND gate. The pSTVAL* line connects to pin 1 of this gate and prevents a write from taking place until the address lines are stable. The inverted pSYNC, at U235 pin 2, ensures that a pulse does not occur on the pWR* line before data is valid on the D0 bus.

CDSB* and MWRT, pins 19 and 68 (control disable and memory write). These lines are not control output lines but are associated with them.

Asserting the CDSB* line 3-states U180 to disconnect the bus control lines. This situation can happen if another CPU board that is plugged into the S-100 bus takes control of the bus. If so, that board must supply the output control signals.

While pWR* is a generalized write strobe for both memory and output ports, MWRT is a write strobe for memory write cycles only. In the Computer, it is used in the memory circuits and on the video board. This signal is derived by NORing pWR* and sOUT (from the status circuits) at U216C.

CIRCUIT DESCRIPTION

Memory

Memory Control Latch

The memory control latch, U176, determines the addressing of RAM and ROM. It also sets the status of the parity circuits.

The CPU accesses this latch by writing the correct byte to port 0FCH. This is done by asserting the $\overline{\text{MEMCTRLCS}}$ line at U159-11 in the I/O port decoder. This signal is then applied to U221D-13, an OR gate.

The CPU next places the data byte to the D inputs of U176, a hex D-type flip-flop, and then asserts pWR* on the S-100 bus. U214-3 couples this control signal through U214-3 to U221-12 and drives U221-11 low.

When the data byte on the D-inputs of U176 has had time to stabilize, U221-11 goes high; clocking the data bus signals into U176 on the positive-going edge.

The bit pattern that was on the data bus is now latched onto the Q outputs of U176, setting the type of memory map addressing (MAPSEL0 & MAPSEL1), monitor ROM addressing (PROM0 & PROM1), and parity operation ($\overline{\text{ZEROPAR}}$ & $\overline{\text{KILPAR}}$).

See the appropriate circuit description and the block diagram description to see how these circuits are affected.

Dynamic Memory

General

The dynamic memory consists of five major circuits: (1) the memory itself, which can be 64K, 128K, or 192K; (2) the address multiplexer, used to convert the 16-bit address bus to the 8-bit address bus required by the dynamic RAMs; (3) the memory map decoder, used to select the correct 64K bank of memory within 192K; (4) the refresh circuits; and (5) the parity circuits.

Dynamic RAM

The Computer uses 64K × 1 bit dynamic RAM chips for main memory. There is one IC per bank per bit position, so that eight ICs make up 64 kbytes. For the first 64K bank, U109 = MD0 and U102 = MD7.

Three sets of these RAMs make up the 192K address space:

U109-U102 = 1st 64K
U125-U118 = 2nd 64K
U145-U138 = 3rd 64K

To read or write memory, the address circuits select the correct RAM location by placing the lower eight bits of the address onto lines MA0-MA7. One of the three RAS lines, 0-2, asserts to latch this address into RAM. The upper eight bits of the address are placed onto MA0-MA7. After waiting a short time for the lines to settle, the CAS lines assert to latch the byte at MD0-MD7 into RAM.

When memory is being read, pin 3 of all the RAM chips are logic 1. This places the addressed data onto pin 14 of each RAM chip. U110 pin 12 then enables U133 to couple this data to the S-100 bus and to the CPU.

If it is writing memory, the CPU enables U132 at pins 1 and 11. U132 couples the data from the S-100 bus to pin 2 of each RAM chip. U110 pin 13 asserts $\overline{WE}$ at pin 3 of each RAM chip to latch the data into the addressed memory location.

CIRCUIT DESCRIPTION

Memory

Address Multiplexer

The address multiplexers consist of U146 and U128. These ICs couple the lower eight bits of the 16-bit address bus to MA0-MA7 during RAS time. They next pass the upper eight bits during CAS time. Multiplexing permits keeping the pin count down on the RAM ICs.

When the CPU starts to access memory, line TAP1 is logic 0. This couples the A-inputs of the multiplexer to the Y-outputs at MA0-MA7. These lines now hold the lower eight bits of the 16-bit address bus. U110, in the memory map circuits, generates a $\overline{\text{RAS}}$ signal to latch this address into RAM.

Forty nanoseconds later, TAP1 goes high. This couples the B-inputs of the multiplexer to MA0-MA7, which are the upper eight bits of the address.

Forty nanoseconds after TAP1 asserts, TAP2 at pin 5 of U110 goes high. This clocks MA0-MA7 into the CAS latches.

Another line going to the multiplexers is $\overline{\text{BCYC}}$. This line is low to indicate that a bus cycle is taking place. The memory is going through a bus cycle whenever the CPU is accessing the memory. $\overline{\text{BCYC}}$ asserts pin 15 of each multiplexer IC to activate their outputs.

If a memory refresh is taking place, $\overline{\text{BCYC}}$ is high and tri-states the multiplexers. At the same time, it activates the outputs of U126, part of the refresh address generator. U126 places a refresh address on MA0-MA7. All three RAS lines assert to refresh the same location in each 64K bank.

If the CPU attempts to read or write memory during refresh, the refresh circuits place the CPU into a wait state until refresh is complete. (See "Refresh Circuits," Page 2-49.)

Memory Map Decoder

The memory map decoder is made up of U111, U110, and U173. It performs three major functions: (1) decodes the address bus to select the correct 64K bank, (2) provides read/write control lines for the RAM and the data bus, and (3) performs correct addressing and control during refresh. These functions are performed as explained below.

U111 selects the correct 64K bank for any memory address below 192K. The address is determined by the map select lines and BA16 and BA17. The map select lines will be covered later. For now, assume the standard configuration (MAPSEL0 = MAPSEL1 = 0; contiguous RAM from 0 to 192K).

Under normal operation, BA16 and BA17 select the banks as follows:

BA17	BA16	Condition
0	0	0 to 64K, $\overline{\text{REN0}}$ asserted.
0	1	(64K + 1) to 128K, $\overline{\text{REN1}}$ asserted.
1	0	(128K + 1) to 192K, $\overline{\text{REN2}}$ asserted.
1	1	U111 disabled.

The last condition is necessary because BA17 allows addressing up to 256K. Since there is no on-board RAM between 192K + 1 and 256K, U111 must be disabled. However, this does not prevent filling this memory range with a 64K board on the S-100 bus.

Also, U111 is disabled if the CPU addresses a location above 256K. In this case, the $\overline{\text{DECODEN}}$ line at pin 14 goes high to place all of U111's outputs to logic 1. $\overline{\text{DECODEN}}$ is controlled by U173 and will be discussed later.

$\overline{\text{BSEL}}$ at U111 pin 9, asserts whenever $\overline{\text{REN0}}$, $\overline{\text{REN1}}$, or $\overline{\text{REN2}}$ asserts. This line is used in the refresh circuits and will be discussed later.

CIRCUIT DESCRIPTION

Memory

The three row-enable lines connect to pins 1, 2, and 3 of the PAL at U110. This IC decodes these, and other inputs, to assert $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and MDGATE at the appropriate times.

Basically, RAS asserts under the Boolean condition: $\overline{RASn} = (RENn*TAP1) + (\overline{RENn*STC*RREQ}) + (\overline{BCYC}*TAP1)$. CAS asserts when: $\overline{CAS\text{-}A} = \overline{CAS\text{-}B} = \overline{CAS\text{-}C} = (\overline{BCYC*TAP2*WO}) + (\overline{BCYC*TAP2*PHANTOM})$.

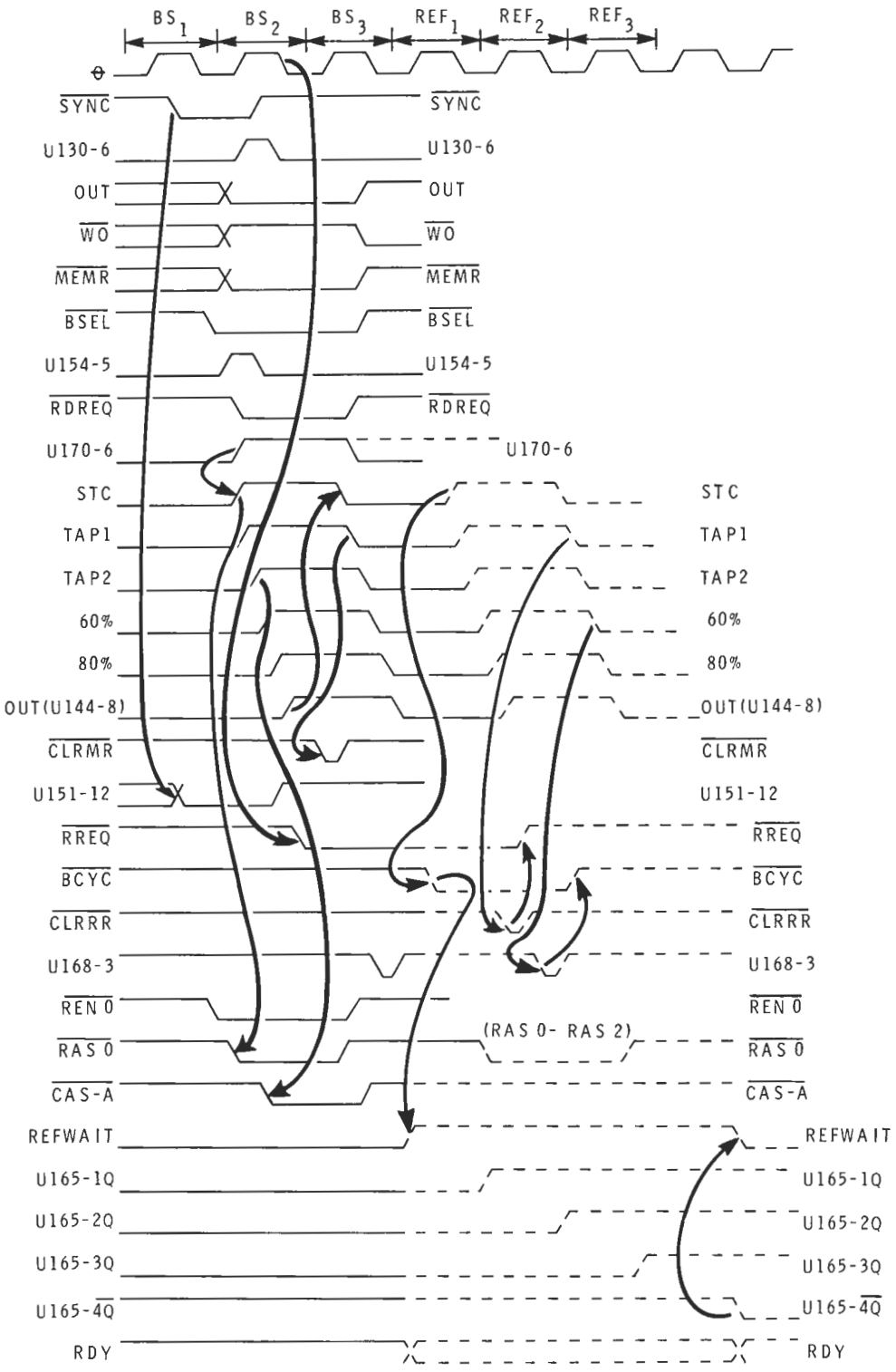
The PHANTOM line permits placing other memory devices into the same address space as the dynamic RAM. When PHANTOM is asserted, the CPU can access the alternate memory device without disturbing the on-board memory. For CAS in the read mode, the addressed memory location is placed on the memory outputs but does not reach the S-100 bus. This is because $\overline{DIEN}$ is logic 1 on U133 pin 1, tri-stating this buffer. During memory write, PHANTOM prevents $\overline{WE}$ from asserting, causing a dummy read cycle.

Refer to the timing diagram in Pictorial 2-10 as the basic timing cycle is discussed.

Assume that the CPU is addressing a location in the first 64K of memory. STC goes high during bus cycle 2; TAP1 = 0 so the logic 0 on $\overline{REN0}$ couples to U110 pin 9, the $\overline{RAS0}$ signal. The lower eight bits of the address are latched into RAM ICs U102-U109.

Forty nanoseconds later, TAP1 goes high. This line causes the address multiplexers to place the upper eight bits of the address onto lines MA0-MA7.

In another 40 nS, TAP2 goes high, causing the CAS lines to assert. The 40-nS delay ensures that the address on MA0-MA7 has had time to settle. Since the 0-64K bank is the only one previously loaded by $\overline{RAS0}$, $\overline{CAS\text{-}A}$ latches the upper eight bits of the address into U102-U109. The other two banks are not affected by $\overline{CAS\text{-}B}$ and $\overline{CAS\text{-}C}$.



Pictorial 2-10
Memory circuit waveforms

CIRCUIT DESCRIPTION

Memory

The memory location pointed to by the address is now written to or read from the CPU. The two remaining outputs of U110 are the write-enable line at pin 13 and the memory data gate at pin 12. Write-enable asserts whenever there is a memory write during a bus cycle at TAP1 or TAP2 time. MDGATE asserts when $\overline{\text{TAP1}}$ or $\overline{\text{BCYC}}$ is asserted. It blocks data from the S-100 bus during a memory write or a refresh operation.

The PAL (U173) is the final IC in the memory map decoder circuits. This IC provides an enable line to U111 ($\overline{\text{DECODEN}}$), an enable line to U133 ($\overline{\text{DIEN}}$) and two reset lines to the refresh circuits ($\overline{\text{CLRRR}}$ and $\overline{\text{CLRMR}}$). These lines have the following definitions:

$\overline{\text{DECODEN}}$, pin 17 (decode enable). This line is normally low for CPU accesses to any memory locations below 256K. If above 256K, one of the extended address lines (BA18-BA23) will be high which will raise $\overline{\text{DECODEN}}$. This, in turn, forces all of the outputs of U111 to go high.

$\overline{\text{DIEN}}$, pin 14 (data in enable). This line enables the outputs of U133 during a memory read to send the addressed data to the CPU. This line goes low when $\overline{\text{DBIN}} = 0$, MDENB = 1, and PHANTOM = 0. MDENB asserts whenever the CPU is accessing the dynamic RAM, which is discussed later. PHANTOM and $\overline{\text{DBIN}}$ are the inverted versions of the S-100 signals, PHANTOM* and pDBIN.

$\overline{\text{CLRRR}}$, pin 16 (clear refresh request). This line resets the refresh request circuits at the end of a memory refresh cycle. This line asserts when TAP1 = 0, TAP2 = 1, and BCYC = 0.

$\overline{\text{CLRMR}}$, pin 15 (clear memory request). This line clears the memory request circuits at the end of a CPU memory read or write cycle. It asserts when TAP1 = 0, TAP = 1, and BCYC = 1.

Refresh Circuits

The refresh circuits consist of a refresh clock, U147-U148; the refresh request circuit, U152; memory request, U167; timing and control ICs U144 and U150; control circuits to the CPU, U168-U158, U150, and U165; and the refresh address generator, U127 and U126.

These circuits refresh the memory when the CPU is not accessing RAM. This is necessary because it is a characteristic of dynamic RAM to lose the contents of its memory if not accessed approximately once every 2 ms.

The refresh circuits contain arbitration logic. If these circuits generate a refresh while the CPU is accessing memory, they wait until the CPU is done before gaining control of the RAM. If the CPU attempts to access memory during a refresh operation, the refresh circuits put the CPU into a wait state until refresh is complete. Also, the refresh circuits provide timing for RAS, CAS, BCYC, and other memory functions for both refresh and CPU operation, as explained below.

U147, a 16-us oscillator, generates the refresh clock. The first negative-going pulse latches U148 pin 5 to logic 1, starting the refresh request. The signal at U168 pin 11 retimes the refresh request to the system clock.

The logic 1 from U148 pin 9 connects to U151 pin 2. Two other lines to this gate must go to logic 1 before the refresh request can take place. They are the start-write ($\overline{\text{STWRT}}$) line in the memory request circuits and the $\overline{\text{SYNC}}$ line from the S-100 bus. If either line is low, then the CPU is about to perform a memory write, or the start of a bus cycle is taking place. As a result, U151 pin 12 stays at logic 0 and a refresh request does not take place.

If $\overline{\text{STWRT}}$ and $\overline{\text{SYNC}}$, are high, SΦ latches U152 pin 5 to logic 1, causing a refresh request. However, the memory circuits do not acknowledge this request if the CPU is executing a memory read cycle. This is because U144 and U150 time

CIRCUIT DESCRIPTION

Memory

the signal so that BCYC (bus cycle active) at U150 pin 9 cannot change to its $\overline{\text{BCYC}}$ state until memory read is completed. This is explained in more detail later.

If, however, no memory read or write is taking place during the refresh request, the logic 0 at U150 pin 12 is latched into U150 pin 9 on the next positive-going signal from U159 pin 3. This signal is generated by the delay line at U144 and is explained in more detail later.

BCYC, now logic 0, 3-states the address multiplexer, U146 and U148, and places the refresh address generator, U127 and U126 onto MA0-MA7. To allow the refresh address generator time to stabilize, U144 delays asserting TAP1 by 40 ns.

Since BCYC is low, U110 in the memory mapping circuits recognizes that this is a refresh cycle. When TAP1 goes high, all three $\overline{\text{RAS}}$ lines assert. This refreshes the entire row pointed to by U126, in each bank.

If the CPU attempts to access memory at this time, U150 through U158 puts the CPU into a wait state. When refresh occurred, $\overline{\text{BCYC}}$ went high to latch U150 pin 5 to logic 1. REFWAIT stays asserted for four clock cycles and is then cleared by the low at U150 pin 1.

If the CPU attempts to write or read memory, $\overline{\text{MEMWR}}$ or MEMR assert at pins 10 and 9 of U170. $\overline{\text{BSEL}}$, at pins 12 and 13 of U130 is also asserted because the CPU has asserted $\overline{\text{REN0}}$, $\overline{\text{REN1}}$, or $\overline{\text{REN2}}$ at U111. Since pins 4 and 5 of U169 are both logic 1, MDENB asserts.

With both MDENB and REFWAIT high, RDY goes low and the CPU goes into a wait state until the refresh cycle is finished, at which time REFWAIT goes low.

MDENB asserts only when the CPU is attempting to access the on-board dynamic RAM. If the CPU is accessing a memory board on the S-100 bus, it will not affect the on-board RAM, so there is no need to put the CPU in a wait state during refresh.

To get an idea of timing relationships, refer to the waveforms in Pictorial 2-10 as you read the following.

Assume that a memory read to an address in the 0-64K range takes place. U154 pin 5 goes high during BS2 because $\overline{\text{MEMR}}$, $\overline{\text{BSEL}}$, and $\overline{\text{SYNC}}$ are asserted. Signal pSTVAL* asserts shortly afterward to clock the $\overline{\text{RDREQ}}$ signal on pin 6 of U167 to logic 0. U169 pin 2 is logic 1, and because pin 8 of U144 is logic 0, pin 1 of U169 is logic 1.

The above process asserts STC and causes signal $\overline{\text{RAS0}}$ on pin 19 of U110 to assert. The lower eight bits on MA0-MA7 are loaded into the RAM's row address latches.

STC also drives U144, a 200-ns delay line with 40-ns taps. TAP1 asserts 40 ns after STC and causes U146 and U128 to place the upper eight bits of the 16-bit address onto MA0-MA7. Forty nanoseconds after that, TAP2 asserts and causes $\overline{\text{CAS-A}}$ to assert at U110, pin 15. Since this is a read cycle, U110 pin 13 is logic 1, and ICs U102-U108 place the addressed data onto pin 14 of each IC. This data is then sent to the CPU through U133.

After TAP2 asserts, the delay line asserts outputs 60%, 80%, and OUT at 40 ns intervals. When OUT goes high, it drives STC low through U166E and U169 pin 1. Forty nanoseconds later, TAP1 goes low to generate a clear memory request pulse ($\overline{\text{CLRMR}}$ = $\overline{\text{TAP1}}$*TAP2*BCYC).

$\overline{\text{CLRMR}}$ clears U174 to drive pin 6 of U170 low, as shown on the solid line on the waveforms, and the read cycle is finished. A write cycle operates in the same manner.

CIRCUIT DESCRIPTION

Memory

Now, assume that a refresh request occurs during the read cycle previously discussed. U148 pin 9 in the request circuits latches high. Also, U151 pin 13 is high since this is not a write operation. However, $\overline{SYNC}$ is low during the first part of the bus cycle, so U151 pin 12 is low.

At the end of SYNC, pin 12 of U151 goes high and pin 5 of U152 (signal RREQ) goes high on the next system clock pulse (end of BS2 on the waveforms). $\overline{RREQ}$ goes low and holds U170 pin 6 high at the end of the read cycle. This is shown as the dashed line in the waveforms.

The low forced on STC by OUT ripples through the delay line and forces STC high during time REF1. This clocks $\overline{RREQ}$ into U150 pin 9, driving BCYC to logic 0. In turn, BCYC 3-states the address multiplexer and places the contents of the refresh address generator into MA0-MA7.

When TAP1 goes high, all three $\overline{RAS}$ lines assert to refresh memory as described previously. The $\overline{RAS}$ lines return high at the end of TAP1 time and U173 asserts the clear refresh request line ($\overline{CLRRR} = \overline{TAP1}*TAP2*\overline{BCYC}$). This resets U148 and U152 in the refresh request circuits. $\overline{CLRRR}$ also increments the refresh address generator at U127, pin 1.

Meanwhile, as the logic 1 ripples through the delay line (shown in dotted lines on the waveforms), the 80% tap is ORed with the inverted 60% tap to pulse U168 pin 3 at time REF3. This places a logic 1 on U150 pin 9, restoring normal bus cycle operation.

The bottom waveforms show what takes place in the ready circuits during a refresh operation. At the start of the refresh cycle, $\overline{BCYC}$ goes high to clock REFWAIT high. The system clock at U165 pin 9 clocks this through to signal $\overline{4Q}$ of U176, which clears REFWAIT at U150, pin 1. The four clock periods that REFWAIT is high mark the time required for the refresh circuits to activate, refresh the memory, and return to their quiescent states.

As described before, if the CPU attempts to read or write the onboard memory during this time, MDENB will go high and force RDY low, generating a wait state. After REFWAIT goes low, RDY goes high, allowing a normal bus cycle to occur.

Note that the refresh circuits do not generate a refresh request every time the CPU is not accessing memory. Refresh happens only once every 16 μs. The CPU is running about 80 times faster than this and can perform many instruction cycles between refreshes. Since the RAMs can go for about 2 ms before requiring refresh, there is no danger of losing memory.

Parity Circuits

The parity circuits consist of U153, U101, U117, U137, and U152. These circuits maintain the parity status for each byte in the 192K of RAM. If a memory location's parity is in error, then the parity circuits send an error signal to the CPU.

U101, U117, and U137, are 64K × 1 RAMs and store 1 bit of parity information for each address location of RAM. These RAMs are addressed by $\overline{RAS}$ and $\overline{CAS}$ in the same way as the other RAMs. However, data transfers take place through U153 instead of the data bus. U153 is a 9-bit odd or even parity generator and checker that processes and maintains the parity status.

During a memory write, the data written into RAM is present at pins 1 through 8 of U153. Pin 14 of each parity RAM is in a high impedance state, so U153 pin 4 is logic 1 through R107.

The following truth table show the levels of the odd and even outputs for the number of high inputs:

CIRCUIT DESCRIPTION

Memory

Number of inputs that are high.	Outputs Even	Outputs Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

So if there is an odd number of high bits in the data byte, the logic 1 on pin 4 of U153 makes the number even. U153 pin 5 responds by going high. If there is an even number of data bits in the data byte, pin 5 of U153 stays low, so the total bit count remains even. U153 pin 5 couples the 1 or 0 through the normally-enabled gate at U151 pin 4 to the data input pins of the parity RAMs.

The $\overline{\text{ZEROPAR}}$ line at U151 pin 5 is normally high. This can be brought low to force all addressed parity RAM locations to 0, regardless of the byte status. It is brought low by clearing data bit D4 to logic 0 and outputting the bit to port 0FCH, the memory control latch. ($\overline{\text{ZEROPAR}}$ is used as a quick test to see if the error-detection circuits work.)

The odd-parity output goes to U152, pin 11. During a memory write, pin 11 is low, preventing an erroneous error signal from being generated. For the same reason, U151 pin 9 remains low for a memory refresh.

During a memory read, data output from the addressed RAMs are present at the inputs of U153. The corresponding parity bit, from U101, U117, or U137, is placed on U153 pin 4. If the bit pattern that was previously written into data RAM and parity RAM has not changed, the total number of high bits is always even. So U153 pin 6 remains low, which is the no-error condition.

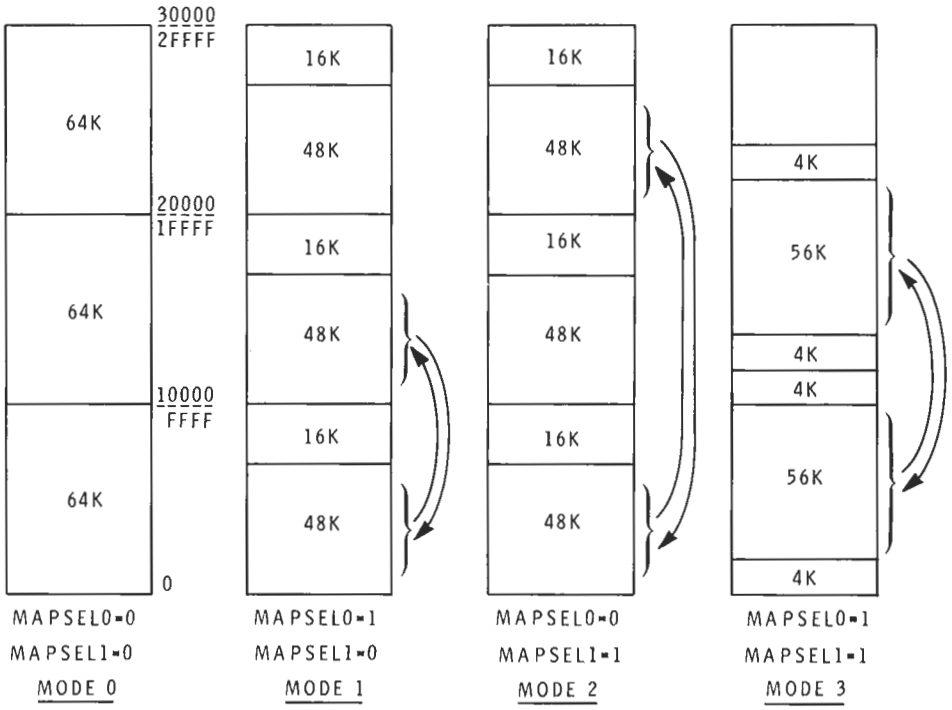
If, however, the bit count is an odd number — due to a chip failure or soft error, for example — then U153 pin 6 goes high. When TAP2 goes low, pin 9 of U152 is latched to logic

1 and asserts the S-100 ERROR* line at U158 pin 6. This generates an error interrupt at U208 pin 18. From here, it is up to the user's software to process the interrupt.

When $\overline{\text{KILPAR}}$ is asserted, U152 is held clear to prevent a parity error interrupt. To assert $\overline{\text{KILPAR}}$, clear data bit D5 to 0 and output it to port 0FCH, the memory control latch.

Map Selection

Map selection takes place at pins 1 and 5 of U111. These two lines, MAPSEL0 and MAPSEL1, also go to pins 7 and 8 of U173, but currently are not used by this IC. Depending on the logic state of pins 1 and 5 of U111, plus the address on lines BA12-BA15, the memory map enters one of the four configurations or modes, shown in Pictorial 2-11.



Pictorial 2-11

CIRCUIT DESCRIPTION

Memory

Mode 0 is the default configuration, in which memory is contiguous from 0 to 192K.

In mode 1, the first 48K of bank 0 appears to be swapped with the first 48K of bank 1. The two 16K areas, and the rest of RAM, are unchanged. This configuration may be used for MP/M* while running the 8085 CPU.

In mode 2, the first 48K of bank 0 appears to be swapped with the first 48K of bank 2. The two 16K areas, and the middle 64K of RAM, are unchanged. This configuration may also be used for MP/M while running the 8085 CPU.

In mode 3, 56K in bank 0 appears to be swapped with 56K in bank 1. Four kilobyte buffers above and below each 56K area remain unchanged, as does the top 64K bank. This configuration would permit using an extended BIOS when running CP/M-2.2* (8-bit operating system software).

Note that, in all cases, the memory only appears to be swapped from the memories point of view. When the CPU addresses the swapped memory, the memory map decoder merely asserts a different RAS line than it normally would.

For example, assume that the Computer is operating in configuration #4. If the CPU should write to the byte at the 6K location, U111 would assert $\overline{\text{REN1}}$ instead of $\overline{\text{REN0}}$. The memory at the 70K location will be written to. Bear in mind, however, that as far as the CPU (and the programmer) is concerned, the byte at 6K was written to.

Address lines BA12-BA15 allow the memory map decoder to keep some sections of memory in place down to 4K increments.

System Monitor ROM

Addressing

The monitor ROM (U190) controls the operation of the Computer after power-up reset or hard reset. It initializes the necessary I/O ports and determines which CPU will be active in the monitor mode. Though currently 8K, jumpers J101 and J102 allow you to expand this ROM to 32K.

Whenever the CPU fetches an instruction from the ROM, it asserts $\overline{\text{DBIN}}$, pin 22, the inverted S-100 pDBIN line. This line comes from U195 pin 16.

The CPU also asserts $\overline{\text{PROMSEL}}$ at U161 pin 15, the ROM-select programmable logic array. This IC changes the memory address that the monitor ROM responds to, effectively repositioning it in memory, as explained below.

After power-up or a hard reset, the memory control latch at U176 is cleared by the reset line at pin 1. This places lines PROM0 and PROM1 of U161 (pins 14 and 17) at logic 0.

When both PROM0 and PROM1 are 0, U161 pin 15 asserts whenever the memory read line asserts at U161 pin 18, no matter what the address. Effectively, the monitor appears to be in all of the address locations.

After a reset, the 8085 CPU is selected by the swap circuits and the 8088 is disabled. The program counter of the 8085 starts fetching op codes starting at address 0 in U190. The monitor causes the 8085 CPU to switch itself off and activate the 8088.

When the 8088 is in control, its program counter starts fetching monitor instructions from memory address FFFF0H, 16 bytes below the top end of the 1 Mbyte address space. However, the ROM still appears to be in all of address space.

CIRCUIT DESCRIPTION

Memory

The 8088 selects the next operating mode by latching PROM1 to logic 1 and leaving PROM0 at logic 0. U190 is now located in the top 8K of the 8088's natural 1 Mbyte address space. This is the location that the ROM is normally in while the Computer is in the monitor mode.

Two other options are available: (1) If PROM0 = 1 and PROM1 = 0, the ROM is placed at the top 8K of every 64K page of memory (this is useful for the 8085, which has only a 64K natural address space); and (2) if PROM0 = 1 and PROM1 = 1, the ROM is disabled.

To select one of the above four options, the CPU must output a data byte to port 0FCH, the memory control latch. Data bit D2 directly affects PROM0 and D3 affects PROM1.

The PHANTOM* Line

The $\overline{\text{PROMSEL}}$ line from U161 also connects to U194, pin 5, an open collector buffer that connects to the PHANTOM* line on the S-100 bus. The PHANTOM* line allows overlapping blocks of memory on the S-100 bus. When properly decoded, the PHANTOM* line disables one block of memory while enabling another.

In this case, whenever the monitor is selected by PROMSEL, the PHANTOM* line goes low and all RAM locations are disabled. Thus, when both PROM0 and PROM1 are 0 at power-up, the CPU reads from ROM but writes to RAM.

Since you can disable the monitor by raising both PROM0 and PROM1 to logic 1, it is possible to have continuous read/write memory from address 0 to the top end of 16 Mbytes (technology permitting). However, you would have to supply your own monitor routine.

Address/Data Circuits

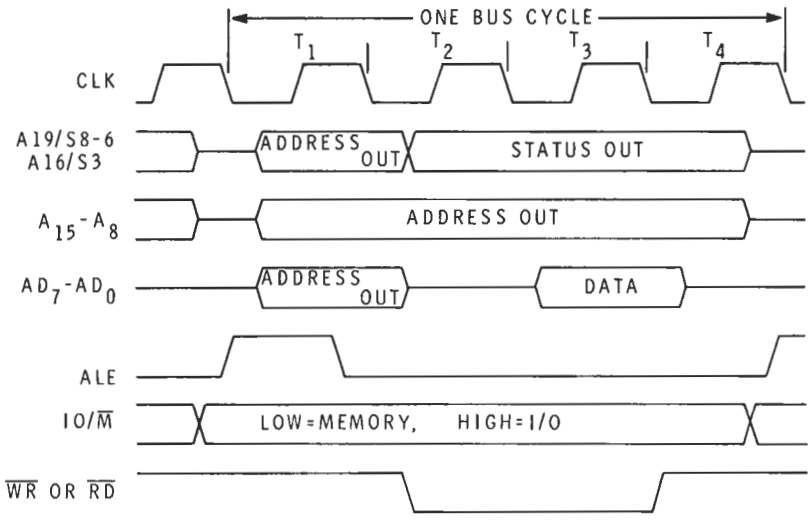
General

Please refer to Pictorial 2-12 while you read the following paragraphs.

As stated in the discussions on the 8085 and the 8088, the address and data lines of these CPUs are multiplexed onto the same bus. That is, first the address is present on the bus, then the data. A control line called the address line enable, or ALE, separates these signals and sends them to their appropriate latches.

Under normal operation, the CPU selection logic enables either the 8085 CPU or the 8088 CPU. Although the address/data lines of these processors are connected in parallel, the bus of the disabled processor is 3-stated, and so does not interfere with the active CPU.

Since the 8085 and 8088 timing diagrams are similar, the 8088 waveforms may be used for the following description.



Pictorial 2-12
iAPX88 Basic Machine Cycle

CIRCUIT DESCRIPTION

Memory

Address Latches

At the beginning of clock cycle T1, the 8088 asserts the 88ALE line at U211 pin 25. This signal couples through the OR gate at U221 pin 1 to pin 11 of U197 and U196, which are two 3-state, octal, D-type latches.

A short time later, the 8088 places address data on the address lines. The lower eight bits, AD0-AD7, go to U197; and the upper eight bits, PA8-PA15, go to U196. These latches are transparent as long as the ALE line is high; that is, the output logic levels are the same as the input logic levels. At the end of T1, ALE goes low to latch the outputs with the address.

The line going to pin 1 of U197 and U196 provides S-100 compatibility, allowing another card to take control of the bus. If an external processor or DMA device were plugged into one of the S-100 slots, and it was to take control of the Computer, it would assert ADSB* low. This would 3-state U197 and U198, thus blocking off the 8085 and 8088.

Data Latches

If the CPU is writing data, either to memory or to an output port, it asserts the $\overline{WR}$ line at U211 pin 29. This signal is inverted by U220 pin 12 to form the CPUWR control signal. CPUWR connects to U198 pin 11 and holds this latch transparent as long as it is high.

During time T3, the CPU places the data on bus lines AD0-AD7, which couple through U198 to its outputs. At time T4, CPUWR goes low to latch this data onto DO0-DO7. From here, the data is sent to the location pointed to by the address on U197 and U196.

U198 pin 1 is the inverted version of DODSB* from the S-100 bus. This signal functions in the same manner as ADSB*.

If the CPU is reading data, either from memory or an input port, its timing is the same as when it writes data. However, this time it asserts the $\overline{RD}$ line at pin 32. This control line is inverted by U220 pin 4 to form RD.

Control line RD connects to U235 pin 11. The other two inputs to U235, $\overline{8259ACS}$ and $\overline{8259ACM}$, are from the interrupt circuits. These two inputs go high when an interrupt occurs. Since RD is high, pin 1 of U217 is low, and this 3-state octal buffer passes the data on bus lines DI0-DI7 to AD0-AD7. At time T3, the CPU assumes that the data is stable and loads it into its accumulator.

CIRCUIT DESCRIPTION

Memory

Extended Addressing

The extended addressing circuits; U193, U212, and U213; maintain S-100 compatibility by making it possible for the CPU to address up to 16 Mbytes of memory.

When the 8088 is active, U193 pin 1 is high and couples PA16-PA19 to pins 3, 4, 7, and 8 of U213. When ALE asserts at U213 pin 11, these address values are coupled over to A16-A19. Lines A20-A23 are logic 0 because the outputs of U212 have not changed from their cleared condition. In this case, the 8088 is operating normally and can directly address its natural 1-M range.

To access the address space above 1M, the CPU asserts $\overline{\text{HI-ADCS}}$ from the I/O port decoder (U159 on MB2). Then $\overline{\text{CPUWR}}$ is asserted causing U221 pin 6 to go low. Finally, the extended address is placed on lines AD4-AD7 at U212. (Lines AD0-AD3 are blocked by U193.)

At the end of that cycle, the $\overline{\text{CPUWR}}$ line goes high and latches AD4-AD7 onto the outputs of U212.

At the beginning of the next machine cycle, when ALE again asserts, the outputs of U212 latch into U213. For example, if U213-12 is logic 1 and pins 15, 16, and 19 are 0, the CPU is in the 1- to 2-M range.

These circuits work the same way if the 8085 is the active CPU. The only difference is that 88SELD at U193 is low so that the lower four bits of U212 couples directly to U213. This allows the 8085 to address memory between 64K and 1M.

Note, however, that once the CPU jumps to these higher ranges it cannot return unless there is a program there to tell it to return. This is because U212 and U213 are latches and can only be changed by software that writes to the high-address port (or through a hard reset). One way around this is to preload a program in higher memory by using direct memory access.

CIRCUIT DESCRIPTION

Interrupt Circuitry

General

Maskable interrupts are routed through the IC at U208, an 8259A programmable interrupt controller (PIC). This IC features an 8-level priority controller and programmable interrupt modes that allow using this IC with either the 8085 or the 8088. Also, individual interrupt lines can be masked without affecting those above or below it. (See the 8259A data sheets in Appendix C for detailed information.)

Before the 8259A can be used, the CPU must initialize it. The CPU does this by outputting the programming information to ports 0F2H and 0F3H for the master, and to 0F0H and 0F1H for the slave. When it accesses these ports, the I/O port decoder asserts $\overline{8259ACSM}$ for the master PIC (U208), and $\overline{8259ACSS}$ for the slave PIC (U209). In addition, it asserts BA0 to select the desired register inside the IC. Once the data to be written has settled on the data pins, D0-D7, the CPU asserts the $\overline{CPUWR}$ line at pin 2 to perform the write.

To read the status registers of the 8259A, the CPU performs the same steps as described above, except it asserts the $\overline{CPURD}$ line at pin 3.

CIRCUIT DESCRIPTION

Interrupt Circuitry

As previously mentioned, U208 is the master PIC and handles all of the main board and video board interrupts. These interrupts are shown in the chart below in order of priority (highest first).

Level	Description
0	ERRORINT: Parity error or S-100 pin 98 (error line).
1	SWAPINT: Processor swap interrupt.
2	TIMRINT: Programmable timer interrupt (Out 0 or Out 2).
3	SLAVE: S-100 vectored interrupt from the 8259A slave IC at U209.
4	EPCIAINT: Serial port A interrupt.
5	EPCIBINT: Serial port B interrupt.
6	KEYINT or DSPYINT: Interrupt from the keyboard , vertical sync, or light pen circuits.
7	$\overline{\text{PRINTINT}}$: Interrupt line from the parallel printer port.

Maskable Interrupt Sequence

Whenever one or more of these lines goes high, U208 evaluates its priority and sends an interrupt request to the CPU through U158 pin 8. The 8259A also asserts the INT* line if the CPU is currently processing a lower-priority interrupt.

Assume that a master interrupt has occurred; that is, one of the interrupt lines other than pin 21 of U208 (INT3) has been asserted. If the CPU does not have masked interrupts, it responds in one of two ways, depending on whether the active processor is the 8085 or the 8088.

If the 8085 is active, the following sequence occurs:

1. The CPU asserts the $\overline{\text{INTA}}$ line at pin 26 (of 8259A).

2. U208 places the 8080/8085 CALL instruction (0CDH) onto the data bus at pins 4 through 11.

3. The 8085 decodes this call instruction and determines that it requires two more bytes. It then sends two more $\overline{\text{INTA}}$ signals to U208.

4. When U208 receives the second $\overline{\text{INTA}}$, it sends the low byte of the vector address to the CPU. When it receives the third $\overline{\text{INTA}}$, it sends the high byte of the vector address to the CPU. (The vector addresses must be programmed into the 8259A during the initialization process.)

5. After saving its current location in stack, the CPU jumps to the address supplied by the 8259A to process the interrupt. When it finishes, the CPU returns to the location saved in stack and continues the program it was processing before interruption.

When the 8088 CPU is active, the 8259A responds somewhat differently to an interrupt acknowledge:

1. The CPU asserts the $\overline{\text{INTA}}$ line at pin 26; the 8259A does not respond at this time.

2. The CPU again asserts $\overline{\text{INTA}}$ on the next machine cycle.

3. The 8259A places a byte on D0-D7 that respresents the interrupt type. The interrupt type is an 8-bit number that depends on which interrupt line caused the interrupt.

CIRCUIT DESCRIPTION

Interrupt Circuitry

4. The CPU multiplies the type number by four to find the correct location in the vector table.

5. The CPU saves its current location in stack and loads the addressed vector table data into the code segment register and instruction pointer. It then processes the service routine pointed to by these registers.

6. When it is done, the CPU returns to the program that it was processing before the interrupt took place.

The slave PIC at U209 processes the S-100 vectored interrupt lines. If one of these lines is asserted, U209 pin 17 goes high to cause a level-3 interrupt at U208 pin 21. This, in turn, sends an interrupt request to the CPU through U158C. When the CPU responds, it asserts pin 26 of U208 and U209.

This time, the master does not place the vector information onto the data bus. Instead, it enables U209 through the cascade lines at pins 12, 13, and 15. U209 then places the vector information onto the bus.

If no interrupt request is present at the time the CPU sends its first $\overline{\text{INTA}}$ signal (i.e., the request duration was too short), the 8259A issues an interrupt level 7. Both the vectoring bytes and the CAS lines appear as if an interrupt level 7 was requested.

Nonmaskable Interrupt Sequence

The nonmaskable interrupt cannot be blocked by software. When the rising edge of the NMI pulse is present at the CPU, the processor must finish its current instruction and service the interrupt request.

The NMI circuits consist of U156C, U156B, and surrounding components. There are two signals that couple to these circuits, NMI* and PWRFAIL, both from the S-100 bus.

NMI* is a general S-100 bus nonmaskable interrupt line. It can be used by S-100 boards to signal the CPU of a catastrophic event, such as imminent loss of power, memory error, or bus parity error.

PWRFAIL* is a dedicated line that asserts if system power failure is imminent. If asserted, the line must stay low until the POC* (power-on clear) line is activated. This line is tied to logic 1 through a 4700 Ω resistor on the S-100 bus. Both hardware and software must be provided to use this line. PWRFAIL* can be selected or disabled by the jumper at J104.

CIRCUIT DESCRIPTION

Interrupt Circuitry

Interrupt Routing

The dual-D flip-flop at U202 retimes the maskable interrupt and applies it to U189A and U189B. If the 8085 is the active CPU, U189A couples the interrupt request to U210 pin 10. If the 8088 is active, U189B routes the request to U211 pin 18.

If an NMI occurs while the 8085 is active, U189D sends it to the TRAP input at U210 pin 6. If the 8088 is active, U189C sends the interrupt to U211 pin 17.

If either an interrupt request or an NMI occur, U156B asserts the NMINT line. This works in conjunction with the interrupt mask bit (MSK) in the processor swap port to force the 8088 into the active state. If MSK is low or NMINT is low, then NMINT has no affect; if MSK is high and NMINT is high, NMINT causes U210 to be disabled and U211 to be enabled.

Keyboard

General

The keyboard circuits are designed around the 8041A universal peripheral interface (UPI) at U204. This IC is a dedicated 8-bit microcomputer with internal RAM and ROM. The RAM is 64 × 8 bits while the ROM is 1024 × 8 bits.

The pin-out of the 8041A is described in the following paragraphs. (For more information, see the 8041A data sheet in Appendix C, Pin-Out Description.)

D0-D7, pins 12-19 (data bus). These are 3-state, bidirectional data bus lines used to interface the UPI to the Computer data bus. The CPU uses this bus to read the code of the pressed key, read UPI status information, and to write command words to the UPI.

$\overline{\text{CS}}$, pin 6 (chip-select line). When the CPU addresses the keyboard circuits at ports 0F4H and 0F5H, the I/O port decoder asserts line $\overline{\text{KEYBDSEL}}$. This activates U204.

A0, pin 9 (address line 0). This is an address input used by the Computer to indicate whether the byte transfer to D0-D7 is data (A0 = 0) or a command (A0 = 1). This signal is derived from the buffered address line 0 (BA0) from U161, pin 18.

$\overline{\text{RD}}$, pin 8 (read data line). When this line is asserted, the UPI transfers its internal data to the D0-D7 lines. The CPU can then load this data into its accumulator.

$\overline{\text{WR}}$, pin 10 (write data line). The CPU places data on pins D0-D7 of the UPI. $\overline{\text{WR}}$ is then asserted by the CPU to load the data into U204.

RESET, pin 4 (reset input line). This line resets the UPI's status flip-flops and sets the program counter to 0.

CIRCUIT DESCRIPTION

Keyboard

XTAL1 and XTAL2, pins 2 and 3 (clock lines). These lines provide a 6-MHz crystal-controlled clock to the circuits inside the UPI.

P10-P17, pins 27-34 (keyboard row input). These bidirectional I/O lines are programmed as input lines. They connect to ROW0-ROW7 of the Computer's matrix keyboard. When a key is pressed, a pulse from one of the column lines (see P20-P23) is coupled into one of the row lines. U204 notes which row is being strobed and, by checking an internal counter, when it is being strobed.

By noting when the strobe pulse occurred, the UPI can tell which column was connected to which row when the key was pressed. From this, it can look up the appropriate key code in ROM and send it to the Computer.

T1, pin 39 (test line 1). When a key is pressed, the UPI checks this line to see if the SHIFT key is also pressed. If so, the UPI jumps to a routine that translates the keypress at ROW0-ROW7 to its appropriate shifted code if it has one.

T0, pin 1 (test line 0). When a key is pressed, the UPI checks this line to see if the CONTROL key is also pressed. If so, the UPI jumps to a routine that translates the keypress at ROW0-ROW7 to its appropriate control code if it has one.

P20-P23, pins 21-24 (keyboard column scan strobe). These bidirectional I/O lines are programmed as outputs. P20 and P21 form a binary counter that counts from 0 to 4. These couple to the A and B inputs of U199 and U184, which are two, dual, 2-to-4 line decoders.

P22 connects to the 1C and 2C inputs of the two decoders. When P22 is low, the data at the A and B inputs is routed to the 2Y outputs; when P22 is high, the A and B data is routed to the 1Y outputs.

P23 connects to the 1G and 2G inputs of U199; it is also coupled to the 1G and 2G inputs of U184 after being inverted. When P23 goes low, it selects U199 and disables U184; when high, it does the opposite.

The combination of these four lines effectively turns U199 and U184 into a 4-to-16 line decoder. When the UPI causes these lines to count up from binary 0 to binary 15, each column pulses low once, starting at column 0 and ending at column 15. At that point, the cycle repeats.

P24, pin 35 (keyboard data ready). This bidirectional I/O line is programmed as an output. When the UPI has data to be sent to the CPU, it places the data on D0-D7 and then raises P24 to logic 1. This asserts KEYINT, sending a keyboard interrupt to the CPU.

P27, pin 38 (bell and keyclick). This bidirectional I/O line is programmed as an output. It pulses to generate the bell and key click sounds. U183 NORs this line with P21 to generate the bell. When U183 pin 1 goes low, it triggers the one-shot at U218. U218 pin 1 pulses high for about 200 ms to gate pin 3 of U232, the 1-kHz oscillator, through U231 to the speaker.

To generate a key click, the negative edge of P27 directly fires the one-shot at U218 pin 5. Pin 6 of this IC goes high for about 10 ms to gate U232 through U231 to the speaker. Note that the click line asserts whenever the bell does. However, since both circuits use the same oscillator, the click is not heard.

CIRCUIT DESCRIPTION

Timer and E-Clock

Timer and Clock

Timer

The timer circuit is designed around the 8253-5 programmable interval timer IC at U160.

The 8253-5 consists of three counters, a data buffer bus, read/write logic, and a control word register.

The counters are 16-bit down-counters with separate clock inputs, gate inputs, and outputs. The clock input causes its associated counter to decrement on the negative-going edge of the clock pulse. The gate input disables its associated counter when brought to logic 0. The output line asserts when the counter reaches 0; whether it asserts high or low depends on how its associated counter is programmed.

The read/write logic allows the CPU to communicate with the 8253-5. It communicates through the data bus buffer when $\overline{CS}$ and either $\overline{RD}$ or $\overline{WR}$ are asserted. Address lines A0 and A1 connect the data bus buffer to one of the counters or to the control word register.

If it is connected to one of the three counters, the CPU can load a starting count into the counter, or read the current count as the counter is down-counting. This data can be either 8 bits or 16 bits.

The CPU writes to the control word register to load it with an 8-bit programming byte. This byte selects the counter to be programmed, determines whether the counter is going to count an 8-bit or 16-bit word, and if it is going to count in binary or BCD. In addition, the control byte sets the operating mode of the counter.

The 8253-5 timer has six programmable operating modes. Briefly, these are:

Interrupt on Terminal Count. The output goes to logic 1 when the counter reaches 0 (terminal count).

Programmable One-Shot. Not used since the gate lines are tied to logic 1.

Rate Generator. This is a divide-by-n counter. The output goes low for one clock period, returns high, and counts down the number stored in the counter. When the counter reaches 0, the output pulses low again and the count starts over.

Square Wave Generator. The output remains high for one-half the count in the down-counter, and then goes low for the remaining count.

Software Triggered Strobe. After the mode is set, the output is high. When the count is loaded, the counter begins counting. On terminal count, the output goes low for one clock period.

Hardware Triggered Strobe. Not used because the gate lines are tied to logic 1.

(See the 8235-5 data sheet in Appendix C for detailed hardware and software information.)

The CPU selects the timer whenever it reads or writes port 0E4 through 0E7. These ports select counters 0 through 2 and the control word register, respectively. Line $\overline{8253CS}$, from the I/O port decoder, chip-selects U160 pin 21, while BA0 and BA1 select the internal counter or register.

The $\overline{8253CS}$ line also enables the two OR gates connected to pins 22 and 23 of U160. If the CPU is reading the data in U160, it asserts the $\overline{DBIN}$ line at U113 pin 12. If it is writing to U160, it asserts $\overline{WR}$ at U113 pin 10.

CIRCUIT DESCRIPTION

Timer and E-Clock

The timer is clocked from CNTRCLK, a 250-kHz clock from U192 pin 11. This signal is parallel-connected to the inputs of counter #0 and counter #2 at pins 9 and 18 of U160. The output of counter #0 at pin 11 of U160 couples to the interrupt status latch at pin 11 of U112, and to the input of counter #1 at U160 pin 15. The counter #1 output is not connected, but when the CPU detects an interrupt from counter #0, it can read the current count through the data bus at pins 1 through 7 of U160.

The output of counter #2, pin 17 of U160, only connects to pin 3 of U112, the other interrupt status latch.

Assume that counter #2 of U160 is programmed to operate as a software-triggered strobe and that both status latches have previously been cleared. When counter #2 counts down to 0, U160 pin 17 goes low for one clock period and then goes high again. This positive-going transition latches a logic 1 into U112 pin 5. At the same time, U112 pin 6 goes low to generate a timer interrupt at U175 pin 12.

The CPU responds by asserting the $\overline{\text{TMRSTATCS}}$ line from the I/O port decoder and the data bus input line, $\overline{\text{DBIN}}$. U113 pin 6 goes low to enable U129 at pins 13 and 10. In turn, these two inverters couple the status of pins 9 and 5 of U112 to D0 and D1 of the data bus. The CPU notes that U112 pin 5 has toggled so it processes the interrupt caused by U160 pin 17.

To clear the latch, the CPU again asserts $\overline{\text{TMRSTATCS}}$, places a logic 0 on data line D1, and asserts the write control line, $\overline{\text{WR}}$. U129 couples D1 to U112 pin 1, which forces pin 6 to 1 and pin 5 to 0.

This circuit operates in the same manner for the counter #0 interrupt.

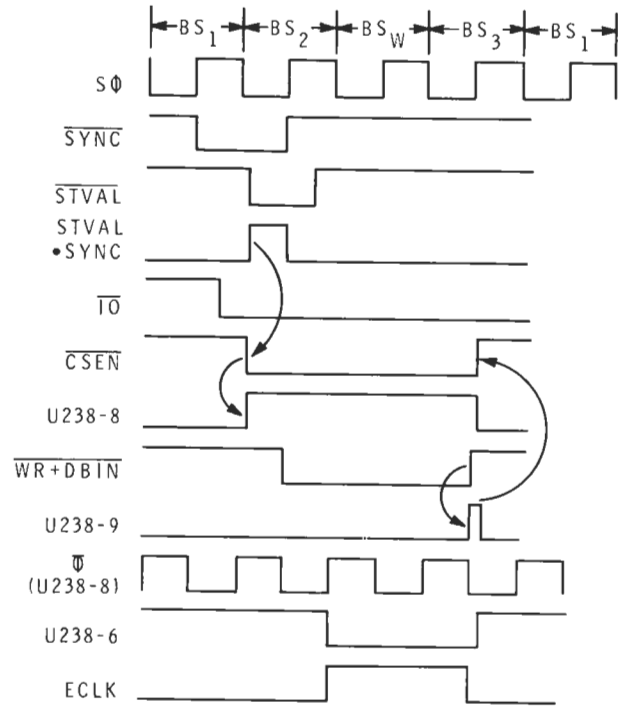
E-Clock

The E-clock logic retimes the S-100 clock and control signals to the values required by the video board and I/O circuits. The timing diagram in Pictorial 2-13 and the following section explains how this is done.

U224 pin 3 forms the STVAL*SYNC signal during bus cycle 2. This provides a status valid signal to the video board. U224 pin 10 generates $\overline{IO}$, a chip-select line to the I/O port decoder and to the video board. The combination of $\overline{IO}$ and STVAL*SYNC form $\overline{CSEN}$ at U238 pin 9. This line provides a chip-enable signal to serial ports A and B.

At the end of the read or write pulse from U224, pin 1, the logic 1 at pin 8 of U238 is latched into pin 9 of U233. This presets U238 pin 9, and brings $\overline{CSEN}$ back to logic 1 during BS3. At the same time, U238 pin 8 goes low to clear U233 pin 9.

During this time, the inverted system clock, $\overline{\Phi}$, works with U238 pin 8 and $\overline{WR*DBIN}$ to form the ECLK signal. This signal provides timing to the parallel port.



Pictorial 2-13

CIRCUIT DESCRIPTION

I/O Circuitry

Serial Ports A and B

General

The two serial ports permit the Computer to communicate with external devices such as printers, MODEMs, plotters, and voice synthesizers. This frees the S-100 slots on the main board for other purposes.

The serial ports are designed around the 2661-2 EPCI (Enhanced Programmable Communications Interface). These ICs have a large number of features, including:

- Polled or interrupt mode operation.
- Asynchronous or synchronous operation.
- 5- to 8-bit characters plus parity.
- Odd, even, or no parity.
- Baud rates from 45.5 baud to 38,400 baud.
- Full handshaking.

(See the 2661-2 data sheet in Appendix D for complete specifications.)

Serial Port A

Serial port A consists of U243 and its surrounding circuitry. This port is a DCE port and can be used to connect to a line printer such as the Z-125AA.

To select this port, the CPU addresses the following ports:

0E8H Receiver holding register (read).
Transmitter holding register (write).

0E9H Status registers (read).
SYN1/SYN2/DLE registers (write).

0EAH Mode registers (read/write).

0EBH Command registers (read/write).

When it selects one of these ports, it asserts $\overline{\text{EPCIACS}}$ from the I/O port decoder and $\overline{\text{CSEN}}$ from the E-clock logic. These lines connect to pins 1 and 2 of U174 and assert the chip-enable line (pin 11) of U243.

Also, the CPU asserts pins 12 and 10 to select the right internal register. The OUT signal at U243 pin 13 determines whether the selected register is written to or read from. This signal is derived from the sOUT signal at U214, pin 14.

The CPU transmits and receives data at lines D0 through D7 on U243. If the CPU is transmitting data, it chip-enables U243, selects the correct register, raises pin 13 of U243 to logic 1, places the data to be transmitted on the inputs of U244, and asserts sWO* at pins 1 and 19 of U244.

The data is loaded into the transmit data holding register inside the EPCI. The EPCI then asserts $\overline{\text{TxRDY}}$ at its pin 15 to raise the EPCIANT line at pin 8 of U222, interrupting the CPU. The CPU responds by not sending any more data until the transmitting holding register is empty.

The EPCI serially transmits the contents of the transmit data holding register out pin 19 and through U245, which converts the TTL to RS-232 levels. In asynchronous mode, the EPCI first sends a start bit; followed by the programmed number of data bits (5 to 8, LSB first), the parity bit (if programmed to send a parity bit), and finally, the programmed number of stop bits, either 1, 1 1/2, or 2.

Once the transmit data holding register is empty, the $\overline{\text{TxRDY}}$ line goes low to inform the CPU that it can send another byte.

CIRCUIT DESCRIPTION

I/O Circuitry

In the receive mode, serial data enters the EPCI at pin 3 through U247D, which converts the + or − 12-volt RS-232 levels to TTL levels. The EPCI extracts the data bits and loads it into the receive data holding register. The $\overline{\text{RxRDY}}$ line then goes low to interrupt the CPU through U222, pin 10. When the CPU processes the interrupt, it addresses U243, places a logic 0 on pin 13, and reads the data at D0-D7 through U241. U241 is selected by asserting the $\overline{\text{BIOSEL}}$ line (from the I/O port decoder) and DBIN at pins 1 and 2 of U222.

The handshake lines are standard EIA RS-232 control lines. These lines are clear to send (CTS), data set ready (DSR), request to send (RTS), and data terminal ready (DTR). To maintain RS-232 standards, they are swapped with their complementary lines at the DCE connector.

Jumpers J109 and J111 allow connecting the DCE RTS line to either $\overline{\text{CTS}}$ or to $\overline{\text{DCD}}$ on the EPCI. If they are connected to the clear to send line, pin 17, the RTS line controls the transmitter. If they are connected to the data carrier detect line at pin 16, RTS controls the receiver.

Depending upon the peripheral, these lines may or may not be used. See the technical manual of the peripheral for that information.

Crystal-controlled oscillator U240 provides a 4.9152-MHz clock to U243 pin 20. The EPCI uses this clock to generate the baud rate frequencies.

Pins 9 and 25 of U243 provide clock to the peripheral device, if it requires it. This timing can be either 1 or 16 times the baud rate. Pins 9 and 25 are connected together since $\overline{\text{TxC}}$ is 3-stated during receive and $\overline{\text{RxC}}$ is 3-stated during transmit.

Serial Port B

Serial port B consists of U242 and its surrounding circuitry. This port is a DTE port and can be used to connect to devices such as a MODEM or to another computer.

To select this IC, the CPU addresses the following ports:

0ECH Receiver holding register (read).
Transmitter holding register (write).

0EDH Status registers (read).
SYN1/SYN2/DLE registers (write).

0EEH Mode registers (read/write).

0EFH Command registers (read/write).

The differences between this port and serial port A are minor. To chip-select this IC, the CPU asserts $\overline{\text{EPCIBCS}}$ instead of $\overline{\text{EPCIACS}}$, the EPCI interrupts the Computer through EPCIB-INT instead of EPCIAINT, and pins 9 and 25 of this port are clock inputs instead of outputs. This last feature is taken care of when the CPU initially programs the EPCI. The frequency can be 1, 16, or 64 times the serial baud rate.

In the asynchronous mode, pins 9 and 25 act as outputs. Under these conditions, D103 and D104 isolate these pins from U247A and U247B.

CIRCUIT DESCRIPTION

I/O Circuitry

Parallel Port

General

The parallel port is designed around a 68A21 peripheral interface adapter (PIA) at U114. This IC performs three functions: (1) it operates as a printer port; (2) it serves as a port for a light pen; and (3) it couples the video board vertical retrace signal to the CPU.

The CPU accesses U114 for programming or data transfer through U135 and U136. At the same time, it chip-selects U114 by asserting the $\overline{6821CS}$ control line from the I/O port decoder. The CPU also asserts address lines BA0 and BA1 (pins 36 and 35) to select the correct internal register.

The enable line, E-CLK, comes from the E-clock logic circuits described previously and provides timing to U114. All other signals to the PIA are referenced to either the rising or falling edges of this line.

The CPU asserts the $\overline{OUT}$ line on pin 21 of U114 when the computer needs to write to the PIA. In all other cases, the PIA is in the read mode when enabled. Actual data transfer between the CPU and PIA takes place when the CPU asserts $\overline{WO}$ at U136 pin 1 for a write, or DBIN at U175 pin 10 for a read. The other connections to U114 are covered in following sections. (For a complete description of the internal operation of the PIA, see the data sheets in Appendix C.)

Printer Port

The printer port is a parallel output port with handshaking capabilities. It allows you to connect the Computer to some of the more popular printers without having to pay extra for a serial interface.

The parallel data leaves U114 at PA0, PA1, and PB2 through PB7 and couples through U115 to J3 where it becomes PDATA1 through PDATA8. J3 couples this data to the printer. When this data is sent, the data is validated by PA2 and the $\overline{\text{STROBE}}$ line goes low to inform the printer that a new byte is present at its input.

The ACKNLG line asserts when the printer has processed the received byte and is ready to receive another character. This signal is inverted by U134A and sent to CB1 on pin 18 of U114. This input can be programmed to detect either a negative-going or positive-going signal, allowing ACKNLG to assert on logic 1 or a logic 0. Some printers handshake when busy.

CB1 detects the voltage transition and asserts the printer interrupt line at U114, pin 37. When the Computer processes the interrupt, it addresses U114's control register to determine which circuit caused the interrupt. When the CPU detects that the printer caused the interrupt, it transmits the next byte to the printer.

The BUSY line asserts if the printer cannot accept a data byte at the time $\overline{\text{STROBE}}$ occurs. This can happen if the print head is moving (such as during a carriage return), if the printer is in the off-line mode, or if an error occurred, such as when the printer runs out of paper.

The BUSY signal is buffered by U116B and couples to CB2 and PA0 on U114. Input CB2 operates in the same manner as CB1 in the ACKNLG circuits. The CPU responds to the interrupt, finds that a printer BUSY signal has occurred, and stops printing until the BUSY line goes to its inactive state.

CIRCUIT DESCRIPTION

I/O Circuitry

To see when the BUSY line goes to the inactive state, it monitors the logic level of PA0. This simplifies programming since, otherwise, CB2 must be programmed to respond to the opposite-polarity signal transition.

The CPU uses the $\overline{\text{INIT}}$ line to initialize some printers. It does this by sending a short pulse (typically 50 ns) to the printer.

The $\overline{\text{ERROR}}$ line asserts if a printer failure occurs, such as when the ribbon needs changing, or when the printer runs out of paper. The CPU stops sending characters until the error is fixed.

Light Pen Port

The light pen circuits consist of U134D, U134B, U134C, U116E, U131, and part of the PIA at U114.

The CPU cannot respond to a signal from the light pen circuits without a user-supplied program to set up interrupts, handle timing, and take care of bit locations detected by the light pen. As a result, this discussion can only be general.

When the CPU lights a dot on the CRT within the range of the light pen, the light pen sends a pulse to U134 pin 5. Jumper J103 allows triggering from either the leading or trailing edge of this pulse. The jumper should be set so that the leading edge always triggers flip-flop U131.

This pulse latches a logic 1 into U131 pin 5, which couples through U116E to the light pen strobe input in the CRT Controller, or CRTC (U330), on the video board. The CRTC saves the address of the byte being accessed. (See the "Theory of Operation" on Page 4.64 in the "Video Board" part of this Manual for more details.)

The output of U131 also couples to pin 40 of U114, a 68A21 peripheral interface adapter. The rising edge of the signal at

pin 40 causes $\overline{\text{IRQA}}$ at pin 38 of U114 to go low if unmasked by software. $\overline{\text{IRQA}}$ is then inverted by pin 13 of U134 to cause a display interrupt at the CPU.

When the CPU acknowledges the interrupt, it must assert the $\overline{\text{6821CS}}$ line (from the I/O decoder port) at U175 pin 4. Line $\overline{\text{6821CS}}$ also chip-selects U114 at pin 23, while BA0/BA1 addresses the PIA control register to see if the light pen circuits generated the interrupt. The $\overline{\text{OUT}}$ line at pin 21 and the DBIN line at U175 pin 10 go to logic 1 to transfer the PIA data to the CPU.

If the interrupt was caused by light pen activity, the CPU processes it according to its program. Before finishing, the CPU clears pin 5 of U131 by pulsing a logic 0 to pin 1 of U131.

U134B, the light pen switch inverter, allows the CPU to monitor the status of a SPST switch connected to LTPNSW at J4. It does this by continually polling PA6 at U114 pin 8. This allows the Computer operator to do such things as move a dot around the CRT face with the light pen. As before, the Computer must be programmed to use this feature.

Video Interrupt Port

The video interrupt port consists of U116G, U131, and U114. The signal at pin 16 of U116, VIDINT, is the vertical sync pulse, VSYNC1D, buffered through pin 9 of U366 on the video board. The CPU times itself from this pulse so that it can update the display during vertical retrace, thus preventing interference on the display. See the "Video Board" circuit description for more details.

When a vertical sync pulse occurs, the positive-going edge from pin 5 of U116 latches a logic 1 into pin 9 of U131. This couples to U114 pin 39, and causes the PIA to generate a display interrupt at U114 pin 38.

When the CPU responds, it checks the PIA control register to determine which line caused the interrupt. Once it finds that VIDINT caused it, the CPU clears U131 by pulsing U114 pin 7 low, and then updates the display circuits as necessary.

CIRCUIT DESCRIPTION

I/O Circuitry

I/O Port Decoder

The heart of the I/O port decoder is U179, a 256 × 4 bit PROM. Depending on which main board port the CPU addresses, U179 enables U159 or U157, respectively a 3-to-8 line decoder and a dual 2-to-4 line decoder.

To address one of these ports (0E0H through 0FFH), the CPU first places the appropriate port address on the inputs of U179, A0 through A7. This address comes from the S-100 address lines, A0-A7, through octal buffer U181.

When the address lines have stabilized, the CPU enables U179 by asserting pin 13, the $\overline{IO}$ line. This signal comes from U224C pin 10 and goes low whenever the CPU asserts the S-100 sINP or sOUT lines. Once $\overline{IO}$ is asserted, U179 decodes the address at its inputs and selects either U159 or U157.

For example, it selects U159 for a memory control latch operation by bringing U179 pin 12 to logic 0. U159 then decodes the lower three bits of the address bus coming in at pins 1, 2, and 3 to assert pin 11, which carries the $\overline{MEMCTRLCS}$ signal.

U159 also selects the following ports:

$\overline{TMRSTATCS}$. This is the timer status port at U160.

$\overline{HI\text{-}ADCS}$. This line controls the extended addressing latches.

$\overline{SWAPCS}$. This line connects to the processor swap port.

$\overline{DWSEL}$. This line controls the power-up reset configuration port at U239.

If U179 pin 11 is asserted, section A of decoder U157 is selected. It decodes address lines BA1 and BA2 to enable the interrupt ports, $\overline{8259ACSS}$ and $\overline{8259ACSM}$, or the keyboard port, KEYBDSEL.

If U179 pin 10 is asserted, section B of decoder U157 is selected. It decodes address lines BA2 and BA3 to enable one of the following ports:

$\overline{6821ACSS}$. The parallel port, U114.

$\overline{8253CS}$. The timer port, U160.

$\overline{EPCIACS}$. Serial port A.

$\overline{EPCIBCS}$. Serial port B.

If the keyboard, serial port A, or serial port B is selected, pin 9 of U179 also goes low. This line is further decoded by U222 to enable U241 whenever the CPU reads data from one of these ports.

REPLACEMENT PARTS LIST

CIRCUIT Comp. No.	HEATH Part No.	Description

Resistors

All resistors are 1/4 W, 5%, unless marked otherwise.

R101-R103	6-472-12	4700 Ω
R104	6-102-12	1000 Ω
R105	6-6651-12	7150 Ω, 1%
R106	6-6811-12	6810 Ω, 1%
R107-R108	6-103-12	10 kΩ
R109-R111	6-102-12	1000 Ω
R112	6-471-12	470 Ω
R113-R114	6-103-12	10 kΩ
R115	6-472-12	4700 Ω
R116	6-154-12	150 kΩ
R117	Jumper wire installed here. No resistor	
R118-R119	6-474-12	470 kΩ
R120	6-224-12	220 kΩ
R121	6-102-12	1000 Ω
R122	6-220-12	22 Ω
R123-R124	6-511-12	510 Ω
R125-R126	6-103-12	10 kΩ
R127	6-102-12	1000 Ω
R128	6-472-12	4700 Ω
RP101	NOT USED	
RP102	9-131	390 Ω, resistor pack
RP103-RP104	9-124	4700 Ω, resistor pack
RP105	NOT USED	
RP106	9-124	4700 Ω, resistor pack
RP107-RP109	9-124	4700 Ω, resistor pack
RP110-RP112	9-132	330 Ω, resistor pack
RP113-RP114	9-124	4700 Ω, resistor pack
RP115	9-132	330 Ω, resistor pack
RP116	9-130	300/390 Ω, resistor pack
RP117	9-133	4700 Ω, resistor pack
RP118	9-124	4700 Ω, resistor pack
RP119	9-106	10 kΩ, resistor pack
RP120	9-128	10 kΩ, resistor pack
RP121-RP122	9-106	10 kΩ, resistor pack
RP123-RP125	9-133	4700 Ω, resistor pack
RP126-RP127	9-106	10 kΩ, resistor pack
RP128	9-128	10 kΩ, resistor pack
RP129-RP130	9-124	4700 Ω, resistor pack

REPLACEMENT PARTS LIST

CIRCUIT Comp. No.	HEATH Part No.	Description

Capacitors

All capacitors are 20%, unless marked otherwise.

C101-C113	21-762	.1 μF ceramic
C113-1	25-918	100 μF electrolytic
C114,C115	21-762	.1 μF ceramic
C116-C118	21-773	470 pF ceramic
C119	21-762	.1 μF ceramic
C120	21-773	470 pF ceramic
C121-C133	21-762	.1 μF ceramic
C134-C138	21-773	470 pF ceramic
C139-C163	21-762	.1 μF ceramic
C164	29-44	.001 μF polystyrene
C165-C173	21-762	.1 μF ceramic
C174	25-924	2.2 μF electrolytic
C174-1	25-918	100 μF electrolytic
C175-C177	21-762	.1 μF ceramic
C178-C179	NOT USED	
C180	25-820	10 μF electrolytic
C181–C185	21-762	.1 μF ceramic
C186	21-718	20 pF ceramic
C187-C188	21-762	.1 μF ceramic
C189	25-918	100 μF electrolytic
C190-C197	21-762	.1 μF ceramic
C198-C199	25-859	.47 μF electrolytic
C200-C202	21-762	.1 μF ceramic
C204-C207	21-762	.1 μF ceramic
C208	25-924	2.2 μF electrolytic
C209	21-762	.1 μF ceramic
C210	29-44	.001 μF polystyrene
C211-C212	21-762	.1 μF ceramic
C213	25-820	10 μF electrolytic
C214-C221	21-762	.1 μF ceramic
C222-C226	21-763	330 pF ceramic

REPLACEMENT PARTS LIST

CIRCUIT Comp. No.	HEATH Part No.	Description
Inductors		
L101-L104	235-229	35 µH
Transducers		
X101	473-29	Audio Transducer
Crystals		
Y101	404-645	10 MHz
Y102	404-647	6 MHz
Y103	404-644	15 MHz
U191	150-132	4 MHz
U240	150-133	4.9152 MHz
Semiconductors		

See "Semiconductor Identification" Page 2.95.

SEMICONDUCTOR IDENTIFICATION

This section is divided into four parts. The "Component Number Index" relates circuit component numbers to Heath part numbers. The "Part Number Index" relates part numbers to manufacturers' part numbers, as well as providing lead configuration drawings for each part. The remaining two parts are "PAL Equations" and "ROM Codes" for the PALs and ROMs on the main circuit board.

Component Number Index

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
D101	57-607
D102-D104	56-56
C203	56-89
U110	444-126
U111	444-104
U112	443-1051
U113	443-875
U114	443-1014
U115-U116	443-791
U117-U125	443-970
U126	443-791
U127	443-973
U128	443-1037
U129	443-811
U130	443-1049
U131	443-1051
U132-U133	443-837
U134	443-872
U135-U136	443-791
U137-U145	443-970
U146	443-1037
U147	442-53
U148	443-948
U149	41-10
U150	443-900
U151	443-864
U152	443-948
U153	443-1001
U154	443-1038
U155	443-728
U156	443-875
U157	443-822
U158	443-1034
U159	443-877
U160	443-1066
U161	444-129-1

SEMICONDUCTOR IDENTIFICATION

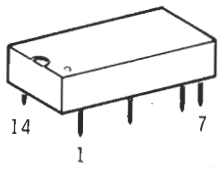
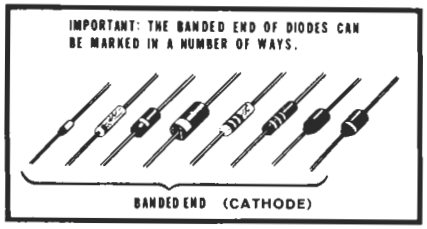
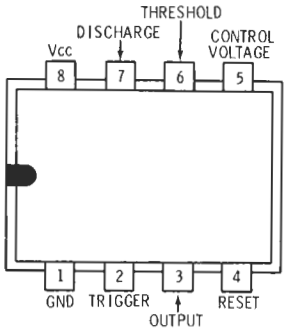
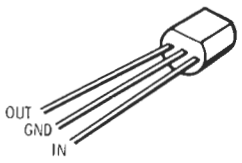
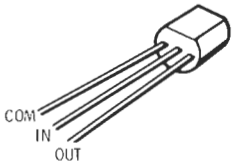
CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
U162-U163	443-791
U164	443-754
U165	443-752
U166	443-872
U167	443-900
U168	443-875
U169	443-976
U170	443-1081
U171-U172	443-1051
U173	444-130
U174	443-875
U175	443-797
U176	443-879
U177	443-754
U178	443-791
U179	444-101
U180	443-857
U181	443-791
U182	443-872
U183	443-779
U184	443-1036
U185	443-872
U186	444-128
U187	443-1051
U188	443-752
U189	443-780
U190	444-87-5
U191	150-132
U192	443-1054
U193	443-857
U194	443-72
U195	443-754
U196-U198	443-837
U199	443-1036
U200	443-1024
U201	443-811
U202	443-1051
U203	443-891
U204	444-141
U205	443-900
U206	443-1045
U207	443-872
U208-U209	443-1012
U210	443-1010
U211	443-1009
U212	443-805
U213	443-837
U214	443-791
U215	443-811
U216	443-1048

SEMICONDUCTOR IDENTIFICATION

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
U217	443-791
U218	443-1112
U219	443-900
U220	443-755
U221	443-875
U222	443-728
U223	443-791
U224	443-1048
U225	443-1049
U226	444-105
U227	443-837
U228	442-644
U229	442-646
U230	443-795
U231	443-74
U232	442-53
U233-U234	443-1051
U235	443-1047
U236	443-1011
U237	443-811
U238	443-1051
U239	443-791
U240	150-133
U241	443-791
U242-U243	443-1061
U244	443-791
U245	443-794
U246-U247	443-795
U248	443-794

SEMICONDUCTOR IDENTIFICATION

Part Number Index

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
41-10	DL14-CB201	200 nS delay line	
56-89	GD510	Diode	
56-56	1N4149		
56-607	1N5817		
442-53	555	Timer	
442-644	78L12	+ 12 V Regulator	
442-646	79L12	– 12 V Regulator	

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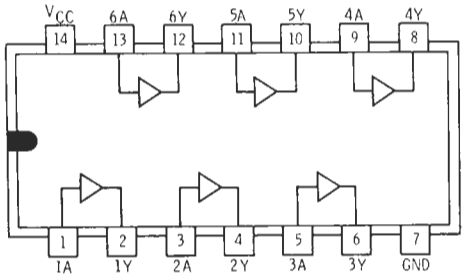
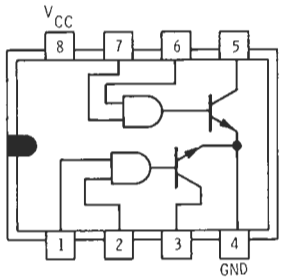
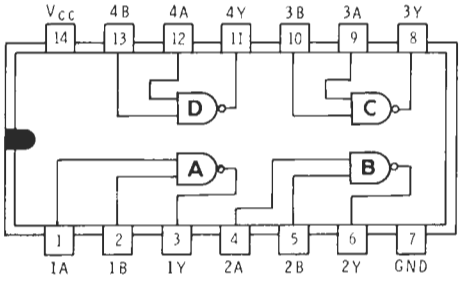
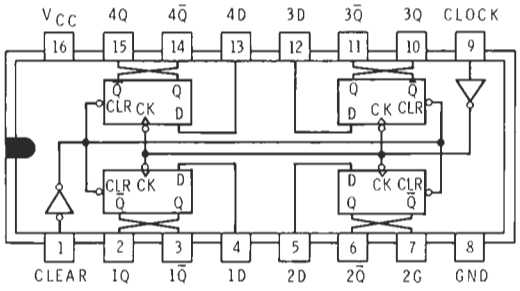
Part Number Index (cont'd)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-72	7417	Open Collector Hex Buffers	
443-74	75452	Peripheral Drivers	
443-728	74LS00	Quad 2-input NAND	
443-752	74LS175	Quad D flip-flop	

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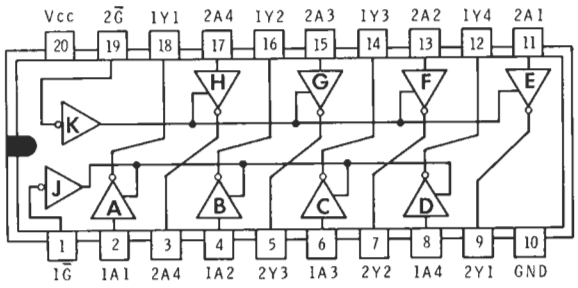
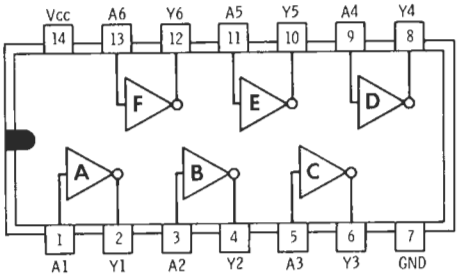
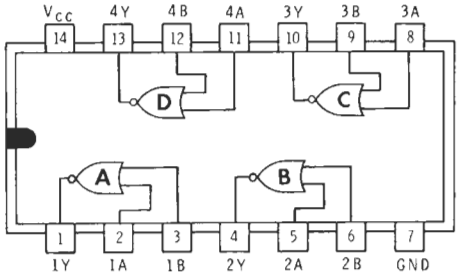
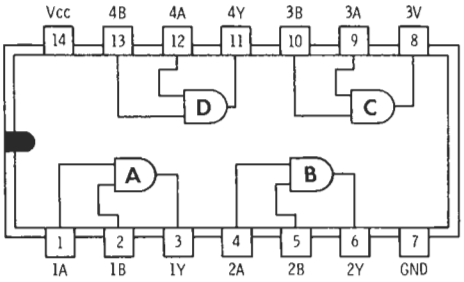
SEMICONDUCTOR IDENTIFICATION

Part Number Index (cont'd)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-754	74LS240	3-state octal Buffer	
443-755	74LS04	Hex inverter	
443-779	74LS02	Quad 2-input NOR	
443-780	74LS08	Quad 2-input AND	

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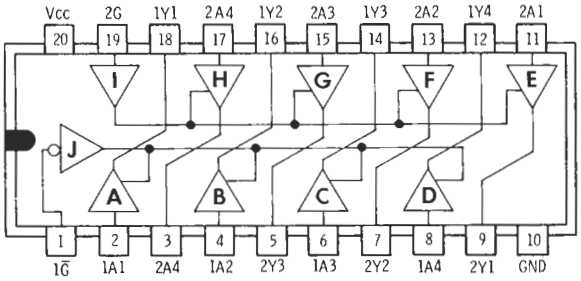
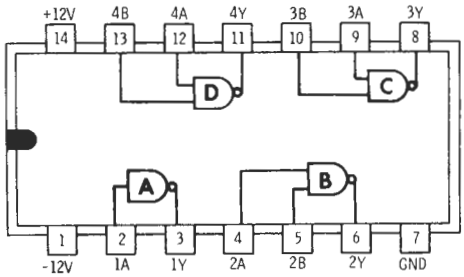
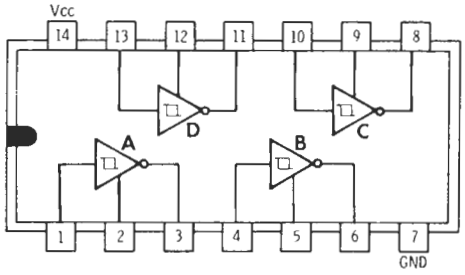
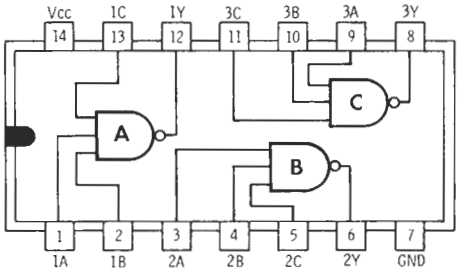
SEMICONDUCTOR IDENTIFICATION

Part Number Index (cont'd)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-791	74LS244	3-state buffer/driver	
443-794	75188	TTL-RS232 driver	
443-795	75189	RS232-TTL receiver	
443-797	74LS10	Triple 3-input NAND	

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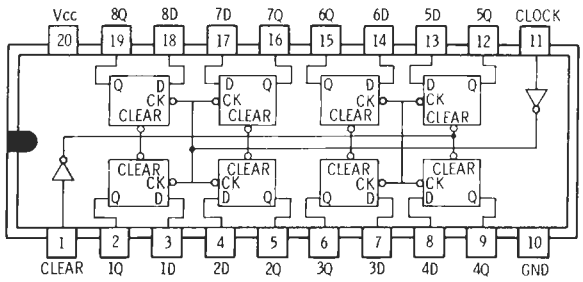
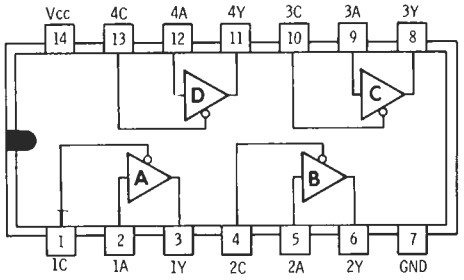
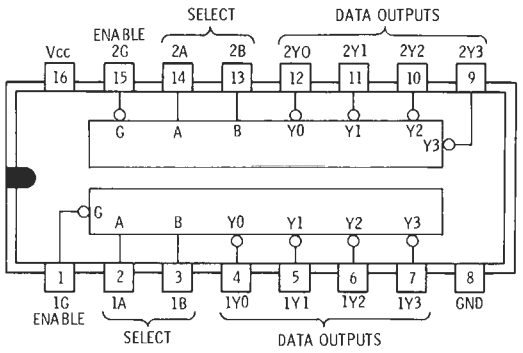
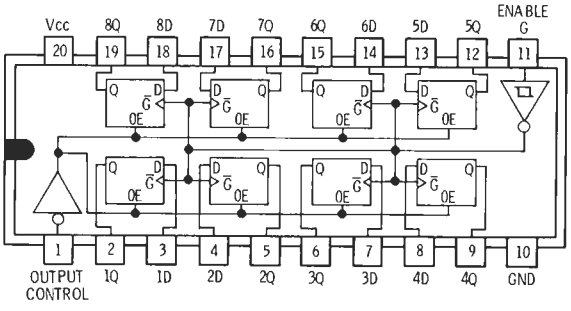
SEMICONDUCTOR IDENTIFICATION

Part Number Index (cont'd)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-805	74LS273	Octal 2-input D flip-flop	
443-811	74LS125	Quad 3-state buffer	
443-822	74LS139	Dual 2 to 4 decoder	
443-837	74LS373	3-state 8-bit latch	

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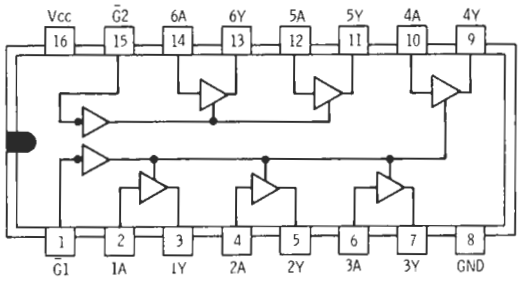
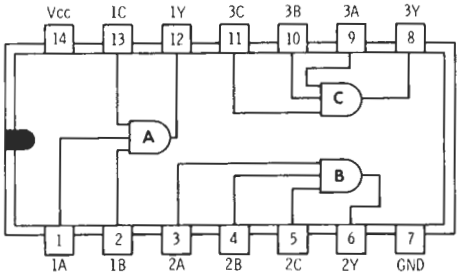
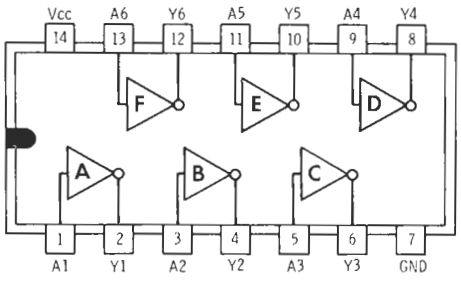
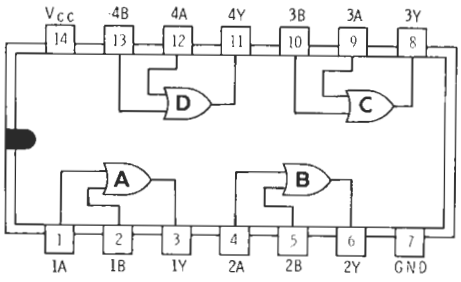
SEMICONDUCTOR IDENTIFICATION

Part Number Index (cont'd)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-857	74LS367	Hex 3-state buffer	
443-864	74LS11	Triple 3-input AND	
443-872	74LS14	Schmitt Trigger Hex inverter	
443-875	74LS32	Quad 2-input OR	

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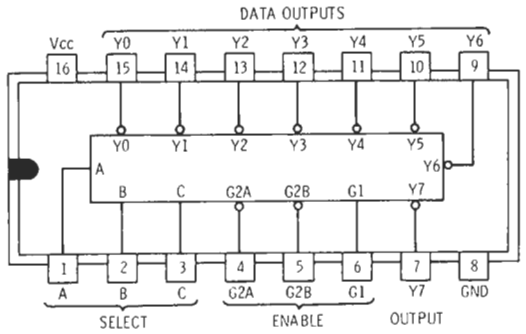
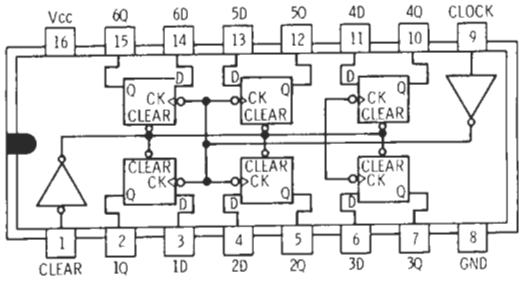
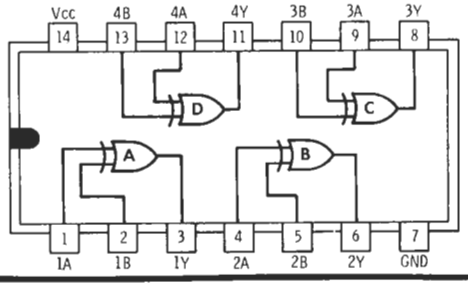
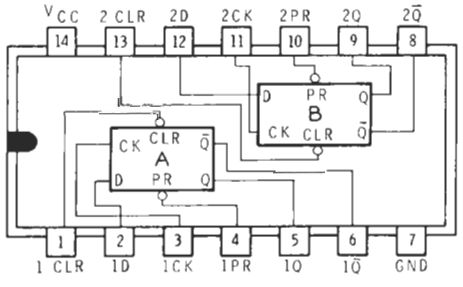
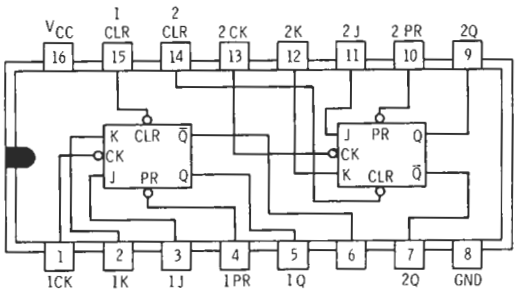
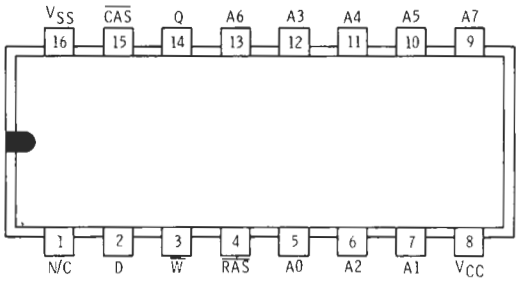
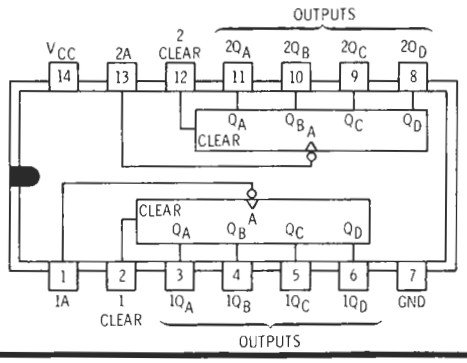
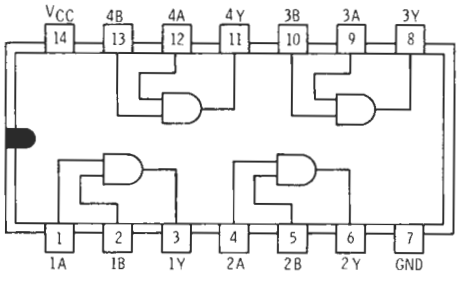
SEMICONDUCTOR IDENTIFICATION

Part Number Index (cont'd)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-877	74LS138	Decoder	
443-879	74LS174	Hex D flip-flop	
443-891	74LS86	Quad 2-input XOR	
443-900	74S74	Dual D flip-flop	

(cont'd)

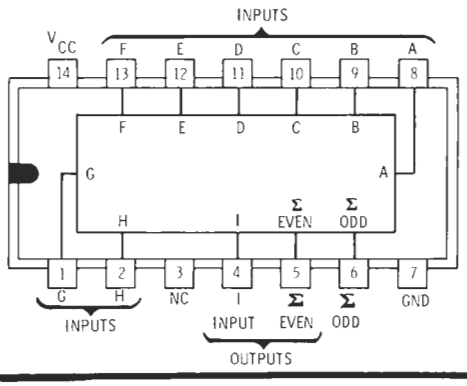
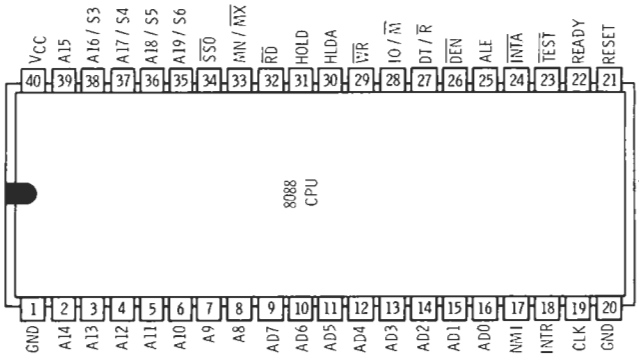
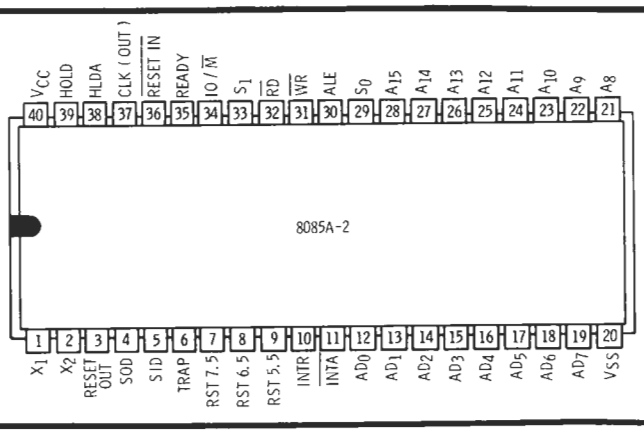
Part Number Index (cont'd)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-948	74LS112	Dual J-K flip-flop	
443-970	MCM6665	64K × 1 RAM	
443-973	74LS393	Binary counter	
443-976	74S08	Quad 2-input AND	

(cont'd)

SEMICONDUCTOR IDENTIFICATION

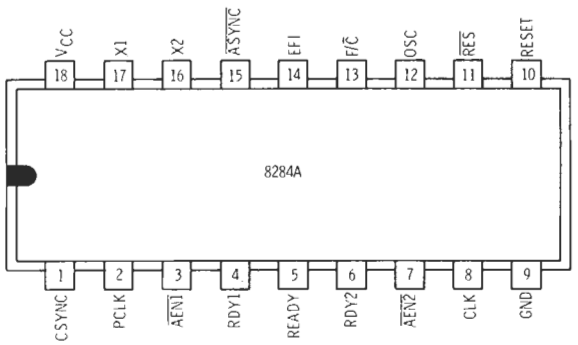
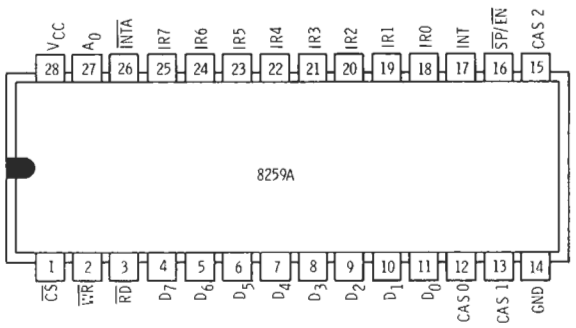
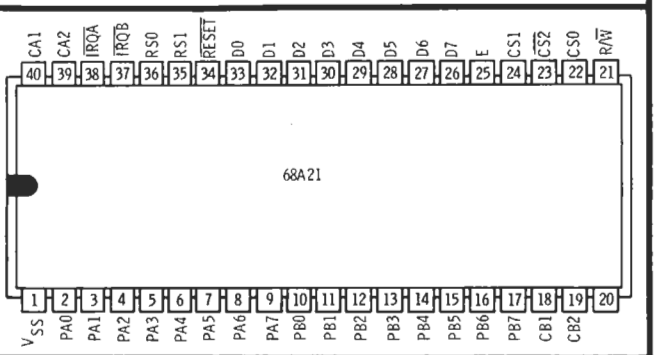
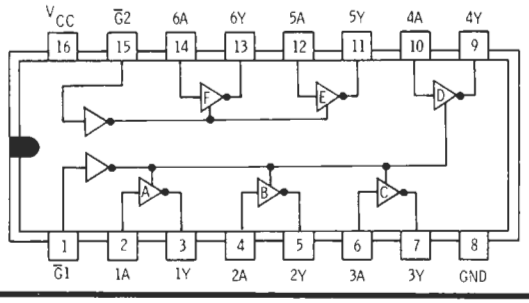
Part Number Index (cont'd)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-1001	74LS280	Odd/even parity check	
443-1009	8088	Microprocessor	
443-1010	8085A-2	Microprocessor	

(cont'd)

SEMICONDUCTOR IDENTIFICATION

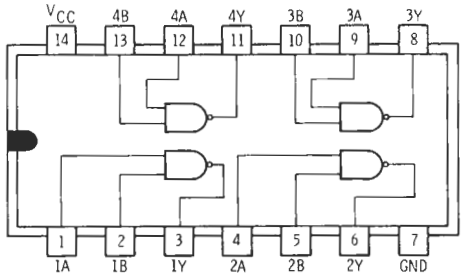
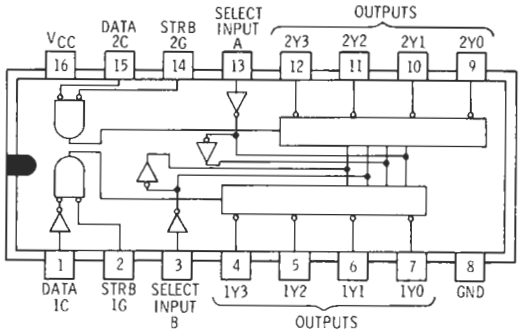
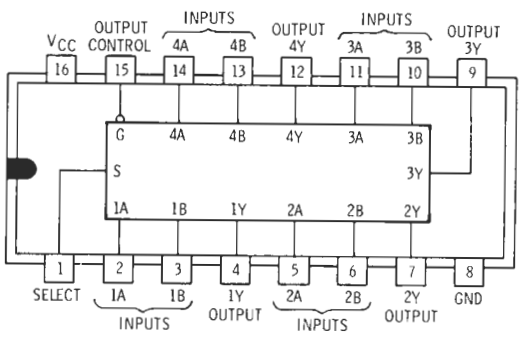
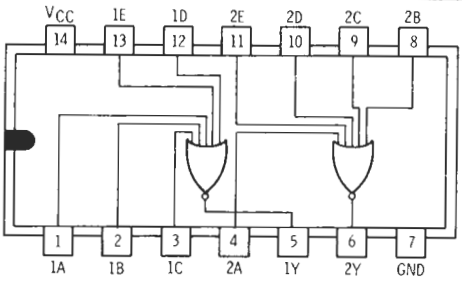
Part Number Index (cont'd)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-1011	8284	Clock Generator/driver	
443-1012	8259A	Programmable Interrupt controller	
443-1014	68A21	PIA	
443-1024	74LS368	Hex 3-state inverter	

(cont'd)

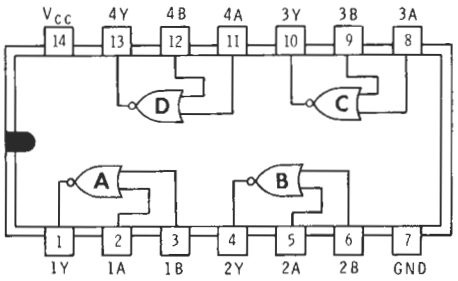
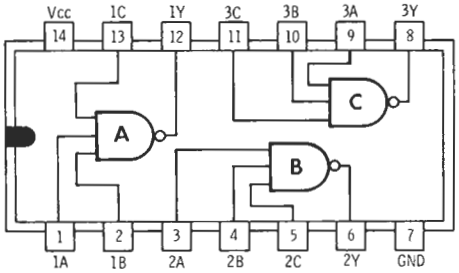
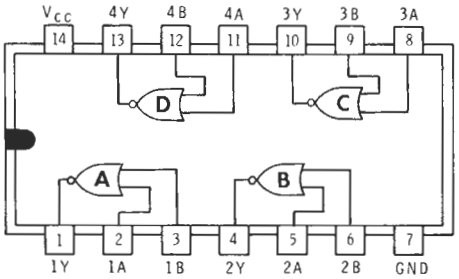
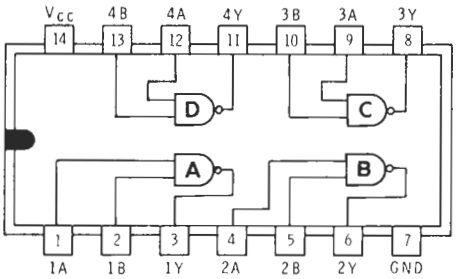
SEMICONDUCTOR IDENTIFICATION

Part Number Index (cont'd)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-1034	74LS38	Quad NAND buffer	
443-1036	74LS156	Dual 2 to 4 decoder	
443-1037	74LS257A	Quad 2 to 1 selector	
443-1038	74S260	Dual 5-input NOR	

(cont'd)

Part Number Index (cont'd)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-1045	74ALS02	Quad 2-input NOR	
443-1047	74ALS10	Triple 3-input NAND	
443-1048	74ALS28	Quad NOR buffer	
443-1049	74ALS37	Quad 2-input NAND buffer	

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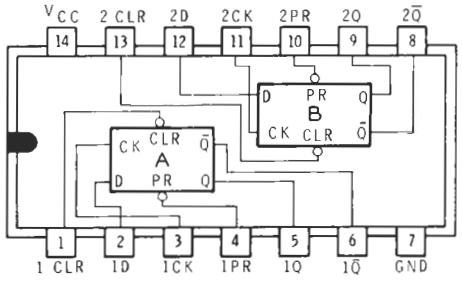
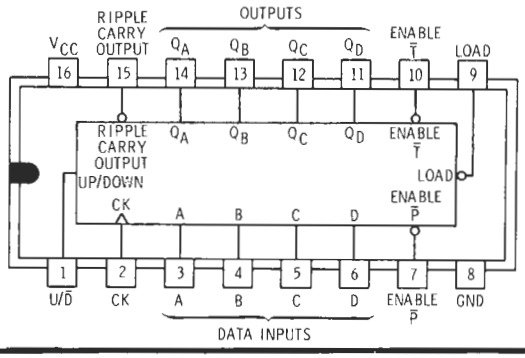
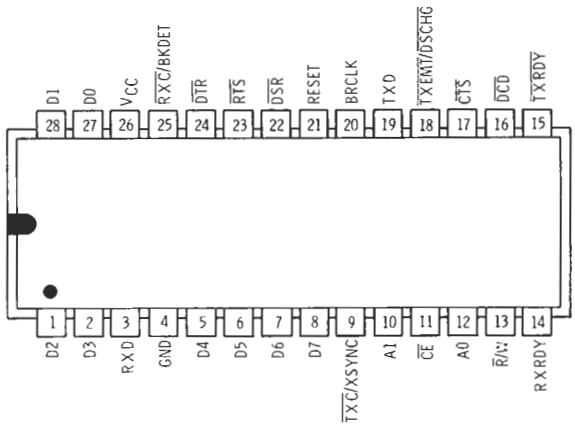
SEMICONDUCTOR IDENTIFICATION

Part Number Index (cont'd)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-1051	74ALS74	Dual D flip-flop	
443-1054	74LS169	4-bit U/D counter	
443-1061	2661-2	EPC 1	

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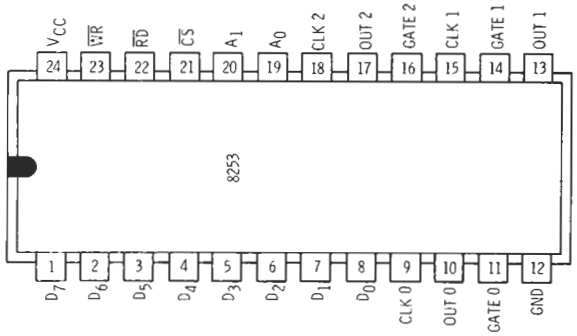
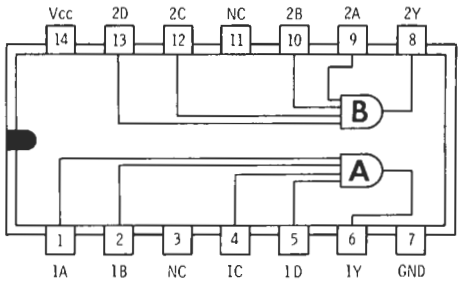
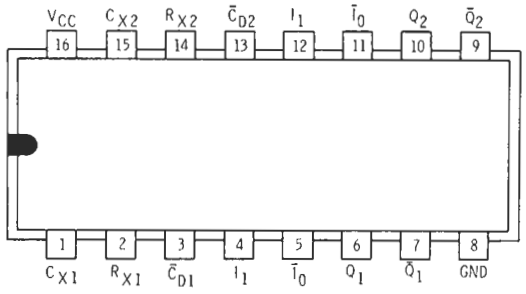
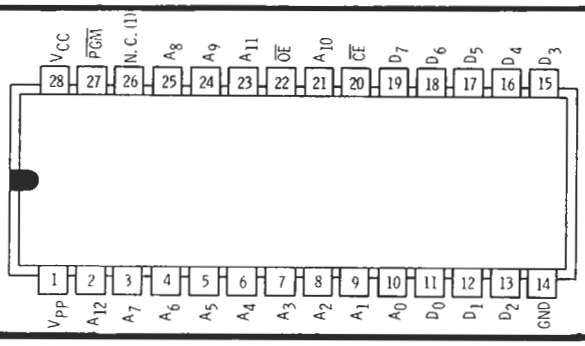
SEMICONDUCTOR IDENTIFICATION

Part Number Index (cont'd)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-1066	8253-5	Programmable interval timer	
443-1081	74ALS1020	Dual 4-input NAND buffer	
443-1112	9602	Multivibrator	
444-87-2	Available only from Zenith Data Systems or Heath Company	8K Monitor ROM	

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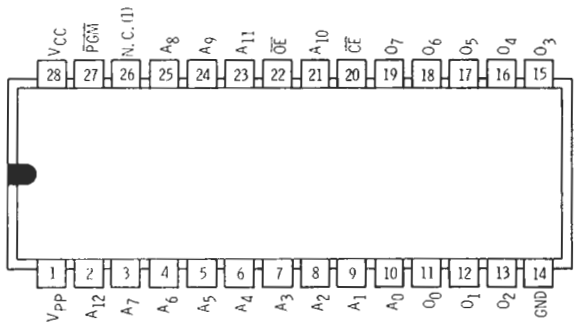
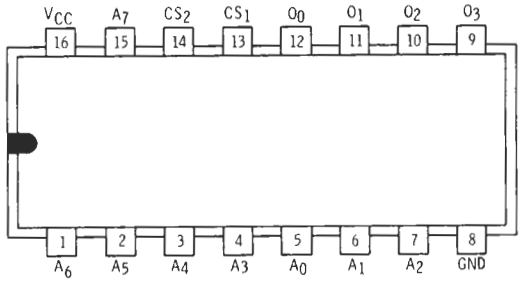
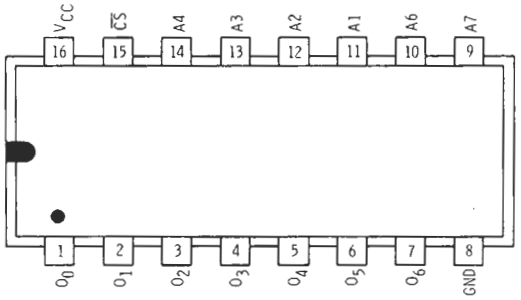
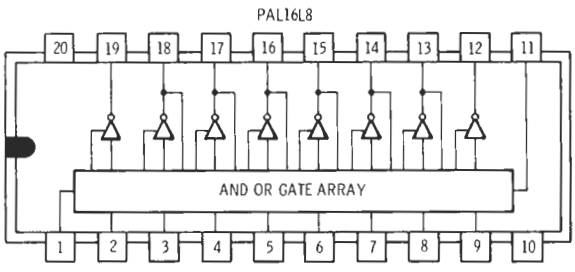
SEMICONDUCTOR IDENTIFICATION

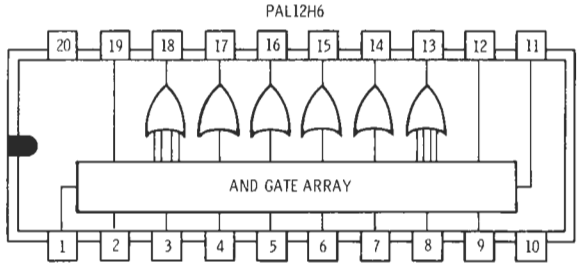
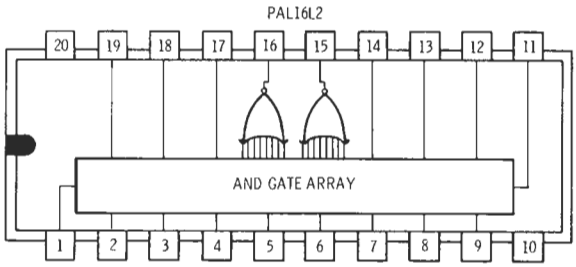
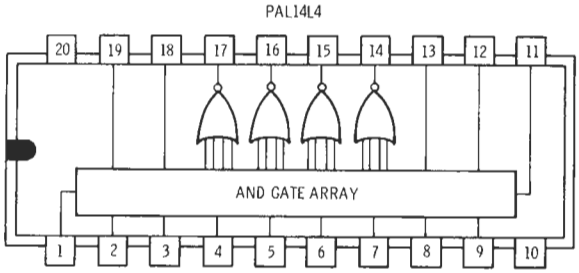
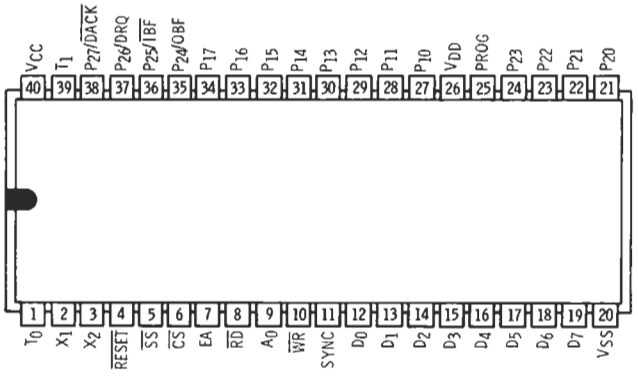
Part Number Index (cont'd)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
444-87-5	Available only from Zenith Data Systems or Heath Company	16K Monitor ROM	
444-101	Available only from Zenith Data Systems or Heath Company	System I/O Decoder ROM	
444-104	Available only from Zenith Data Systems or Heath Company	Memory Decoder ROM	
444-105	Available only from Zenith Data Systems or Heath Company	System status decoder ROM	
444-126	Available only from Zenith Data Systems or Heath Company	HAL or PAL16L8 Memory timing control	

(cont'd)

SEMICONDUCTOR IDENTIFICATION

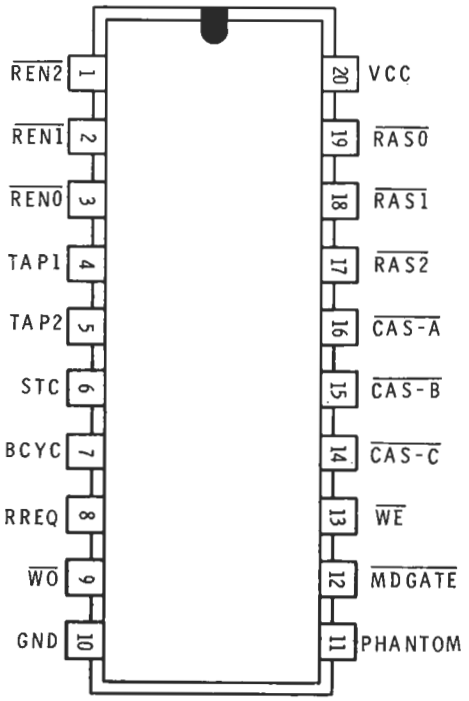
Part Number Index (cont'd)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
444-128	Available only from Zenith Data Systems or Heath Company	HAL or PAL12H6 Processor swap control	
444-129-1	Available only from Zenith Data Systems or Heath Company	HAL or PAL16L2 ROM address decoder	
444-130	Available only from Zenith Data Systems or Heath Company	HAL or PAL14L4 Memory high address decoder	
444-109	8041A	Keyboard processor	
444-141	8741A		

SEMICONDUCTOR IDENTIFICATION

Pal Equations

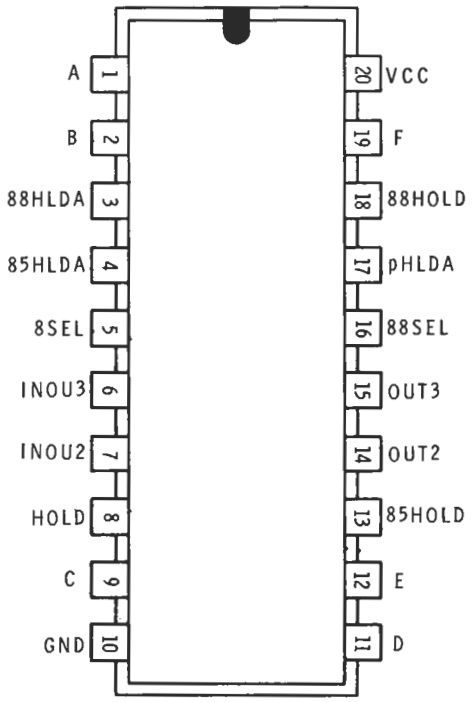
444-126/RAM Controller



LOGIC EQUATIONS

$\overline{RAS0}$ = REN0*TAP1 + REN0*STC* $\overline{RREQ}$ + $\overline{BCYC}$*TAP1
$\overline{RAS1}$ = REN1*TAP1 + REN1*STC*$\overline{RREQ}$ + $\overline{BCYC}$*TAP1
$\overline{RAS2}$ = REN2*TAP1 + REN2*STC*$\overline{RREQ}$ + $\overline{BCYC}$*TAP1
$\overline{CAS\text{-}A}$ = BCYC*TAP2*$\overline{WO}$ + $\overline{BCYC}$TAP2*$\overline{PHANTOM}$
$\overline{CAS\text{-}B}$ = BCYC*TAP2*$\overline{WO}$ + BCYC*TAP2*$\overline{PHANTOM}$
$\overline{CAS\text{-}C}$ = BCYC*TAP2*$\overline{WO}$ + BCYC*TAP2*$\overline{PHANTOM}$
$\overline{WE}$ = BCYC*WO*TAP2 + BCYC*WO*TAP1
$\overline{MDGATE}$ = $\overline{TAP1}$ + $\overline{BCYC}$

444-128/Hold of Dual Processors



LOGIC EQUATIONS

88HOLD = $\overline{85HLDA}$ + $\overline{8SEL}$ + INOU3*HOLD + HOLD* 85HLDA*$\overline{88HLDA}$*8SEL

pHLDA = INOU3*85HLDA*88HLDA

88SEL = 85HLDA*$\overline{88HLDA}$ + 85HLDA*88HLDA*8SEL

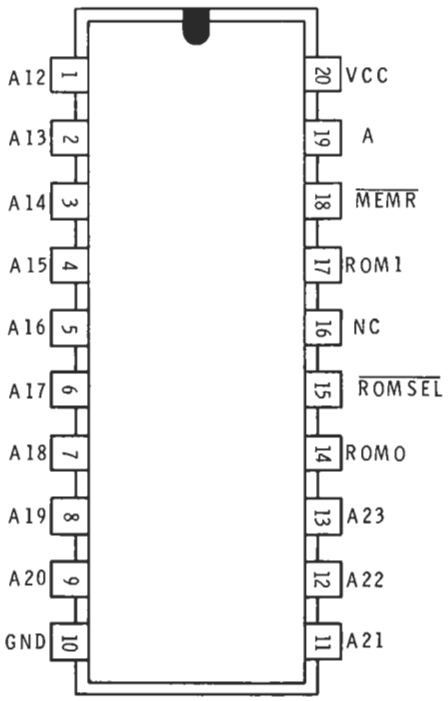
OUT3 = INOU3*85HLDA*88HLDA + INOU2

OUT2 = $\overline{85HLDA}$*88HLDA*$\overline{8SEL}$ + HOLD*$\overline{85HLDA}$*$\overline{88HLDA}$*8SEL

85HOLD = INOU3*HOLD*85HLDA*88HLDA*$\overline{8SEL}$ + HOLD*$\overline{85HLDA}$ *88HLDA*$\overline{8SEL}$ + 85HLDA*$\overline{88HLDA}$ + 88HLDA*8SEL

SEMICONDUCTOR IDENTIFICATION

444-129-1/Top 32K Selector

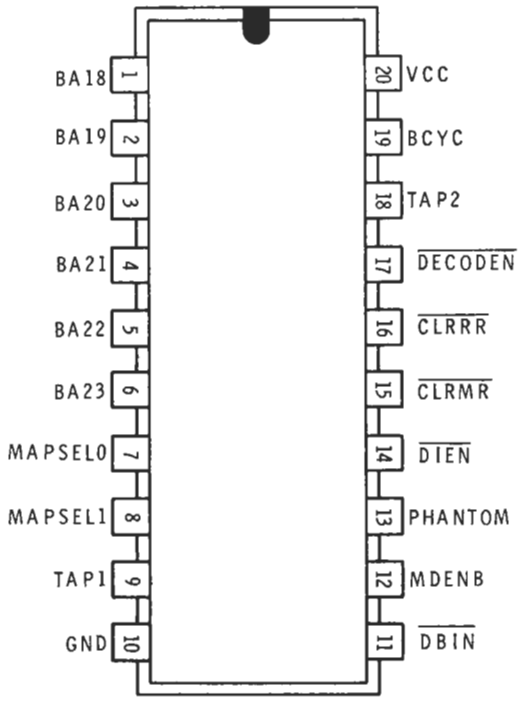


LOGIC EQUATION

$$\overline{ROMSEL} = MEMR*\overline{ROM0}*\overline{ROM1} + MEMR*ROM0*\overline{ROM1}*A15 + MEMR*\overline{ROM0}*ROM1*A15*A16*A17*A18*A19*\overline{A20}*\overline{A21}*\overline{A22}*\overline{A23}$$

SEMICONDUCTOR IDENTIFICATION

444-130/High Address Decoder



LOGIC EQUATIONS

$$\overline{DECODEN} = \overline{BA18}*\overline{BA19}*\overline{BA20}*\overline{BA21}*\overline{BA22}*\overline{BA23}$$
$$\overline{DIEN} = DBIN*MDENB*\overline{PHANTOM}$$
$$\overline{CLRRR} = \overline{TAP1}*TAP2*\overline{BCYC}$$
$$\overline{CLRMR} = \overline{TAP1}*TAP2*BCYC$$

SEMICONDUCTOR IDENTIFICATION

ROM Codes

```
                                        title  IODEC I/O decoder for the Z-100

                                ;       ZDS part no.:   444-101
                                ;       release date:   5/25/82
                                ;               prom:   82s129(256x4)
                                ;           checksum:   0e57

0000'                                   cseg
0010                                    .radix  16
                                        org     0

0000'   0F                              db      0f
0001'   0F                              db      0f
0002'   0F                              db      0f
0003'   0F                              db      0f
0004'   0F                              db      0f
0005'   0F                              db      0f
0006'   0F                              db      0f
0007'   0F                              db      0f
0008'   0F                              db      0f
0009'   0F                              db      0f
000A'   0F                              db      0f
000B'   0F                              db      0f
000C'   0F                              db      0f
000D'   0F                              db      0f
000E'   0F                              db      0f
000F'   0F                              db      0f
0010'   0F                              db      0f
0011'   0F                              db      0f
0012'   0F                              db      0f
0013'   0F                              db      0f
0014'   0F                              db      0f
0015'   0F                              db      0f
0016'   0F                              db      0f
0017'   0F                              db      0f
0018'   0F                              db      0f
0019'   0F                              db      0f
001A'   0F                              db      0f
001B'   0F                              db      0f
001C'   0F                              db      0f
001D'   0F                              db      0f
001E'   0F                              db      0f
001F'   0F                              db      0f
0020'   0F                              db      0f
0021'   0F                              db      0f
0022'   0F                              db      0f
```

IODEC I/O decoder for the Z-100

```
0023'   0F                      db      0f
0024'   0F                      db      0f
0025'   0F                      db      0f
0026'   0F                      db      0f
0027'   0F                      db      0f
0028'   0F                      db      0f
0029'   0F                      db      0f
002A'   0F                      db      0f
002B'   0F                      db      0f
002C'   0F                      db      0f
002D'   0F                      db      0f
002E'   0F                      db      0f
002F'   0F                      db      0f
0030'   0F                      db      0f
0031'   0F                      db      0f
0032'   0F                      db      0f
0033'   0F                      db      0f
0034'   0F                      db      0f
0035'   0F                      db      0f
0036'   0F                      db      0f
0037'   0F                      db      0f
0038'   0F                      db      0f
0039'   0F                      db      0f
003A'   0F                      db      0f
003B'   0F                      db      0f
003C'   0F                      db      0f
003D'   0F                      db      0f
003E'   0F                      db      0f
003F'   0F                      db      0f
0040'   0F                      db      0f
0041'   0F                      db      0f
0042'   0F                      db      0f
0043'   0F                      db      0f
0044'   0F                      db      0f
0045'   0F                      db      0f
0046'   0F                      db      0f
0047'   0F                      db      0f
0048'   0F                      db      0f
0049'   0F                      db      0f
004A'   0F                      db      0f
004B'   0F                      db      0f
004C'   0F                      db      0f
004D'   0F                      db      0f
004E'   0F                      db      0f
004F'   0F                      db      0f
0050'   0F                      db      0f
```

SEMICONDUCTOR IDENTIFICATION

```
IODEC I/O decoder for the Z-100

0051'   0F                      db      0f
0052'   0F                      db      0f
0053'   0F                      db      0f
0054'   0F                      db      0f
0055'   0F                      db      0f
0056'   0F                      db      0f
0057'   0F                      db      0f
0058'   0F                      db      0f
0059'   0F                      db      0f
005A'   0F                      db      0f
005B'   0F                      db      0f
005C'   0F                      db      0f
005D'   0F                      db      0f
005E'   0F                      db      0f
005F'   0F                      db      0f
0060'   0F                      db      0f
0061'   0F                      db      0f
0062'   0F                      db      0f
0063'   0F                      db      0f
0064'   0F                      db      0f
0065'   0F                      db      0f
0066'   0F                      db      0f
0067'   0F                      db      0f
0068'   0F                      db      0f
0069'   0F                      db      0f
006A'   0F                      db      0f
006B'   0F                      db      0f
006C'   0F                      db      0f
006D'   0F                      db      0f
006E'   0F                      db      0f
006F'   0F                      db      0f
0070'   0F                      db      0f
0071'   0F                      db      0f
0072'   0F                      db      0f
0073'   0F                      db      0f
0074'   0F                      db      0f
0075'   0F                      db      0f
0076'   0F                      db      0f
0077'   0F                      db      0f
0078'   0F                      db      0f
0079'   0F                      db      0f
007A'   0F                      db      0f
007B'   0F                      db      0f
007C'   0F                      db      0f
007D'   0F                      db      0f
007E'   0F                      db      0f
```

```
IODEC I/O decoder for the Z-100

007F'   0F                      db      0f
0080'   0F                      db      0f
0081'   0F                      db      0f
0082'   0F                      db      0f
0083'   0F                      db      0f
0084'   0F                      db      0f
0085'   0F                      db      0f
0086'   0F                      db      0f
0087'   0F                      db      0f
0088'   0F                      db      0f
0089'   0F                      db      0f
008A'   0F                      db      0f
008B'   0F                      db      0f
008C'   0F                      db      0f
008D'   0F                      db      0f
008E'   0F                      db      0f
008F'   0F                      db      0f
0090'   0F                      db      0f
0091'   0F                      db      0f
0092'   0F                      db      0f
0093'   0F                      db      0f
0094'   0F                      db      0f
0095'   0F                      db      0f
0096'   0F                      db      0f
0097'   0F                      db      0f
0098'   0F                      db      0f
0099'   0F                      db      0f
009A'   0F                      db      0f
009B'   0F                      db      0f
009C'   0F                      db      0f
009D'   0F                      db      0f
009E'   0F                      db      0f
009F'   0F                      db      0f
00A0'   0F                      db      0f
00A1'   0F                      db      0f
00A2'   0F                      db      0f
00A3'   0F                      db      0f
00A4'   0F                      db      0f
00A5'   0F                      db      0f
00A6'   0F                      db      0f
00A7'   0F                      db      0f
00A8'   0F                      db      0f      ;Reserved for Z-217
00A9'   0F                      db      0f      ;Reserved for Z-217
00AA'   0F                      db      0f      ;Reserved for Z-217
00AB'   0F                      db      0f      ;Reserved for Z-217
00AC'   0F                      db      0f      ;Reserved for Z-217
```

SEMICONDUCTOR IDENTIFICATION

IODEC I/O decoder for the Z-100

```
00AD'   0F                      db      0f      ;Reserved for Z-207
00AE'   0F                      db      0f      ;Reserved for Z-207
00AF'   0F                      db      0f      ;Reserved for Z-207
00B0'   0F                      db      0f      ;Primary      Z-207
00B1'   0F                      db      0f      ;Primary      Z-207
00B2'   0F                      db      0f      ;Primary      Z-207
00B3'   0F                      db      0f      ;Primary      Z-207
00B4'   0F                      db      0f      ;Primary      Z-207
00B5'   0F                      db      0f      ;Primary      Z-207
00B6'   0F                      db      0f      ;Primary      Z-207
00B7'   0F                      db      0f      ;Primary      Z-207
00B8'   0F                      db      0f      ;Secondary    Z-207
00B9'   0F                      db      0f      ;Secondary    Z-207
00BA'   0F                      db      0f      ;Secondary    Z-207
00BB'   0F                      db      0f      ;Secondary    Z-207
00BC'   0F                      db      0f      ;Secondary    Z-207
00BD'   0F                      db      0f      ;Secondary    Z-207
00BE'   0F                      db      0f      ;Secondary    Z-207
00BF'   0F                      db      0f      ;Secondary    Z-207
00C0'   0F                      db      0f      ;    Reserved
00C1'   0F                      db      0f      ;    Reserved
00C2'   0F                      db      0f      ;    Reserved
00C3'   0F                      db      0f      ;    Reserved
00C4'   0F                      db      0f      ;    Reserved
00C5'   0F                      db      0f      ;    Reserved
00C6'   0F                      db      0f      ;    Reserved
00C7'   0F                      db      0f      ;    Reserved
00C8'   0F                      db      0f      ;    Reserved
00C9'   0F                      db      0f      ;    Reserved
00CA'   0F                      db      0f      ;    Reserved
00CB'   0F                      db      0f      ;    Reserved
00CC'   0F                      db      0f      ;    Reserved
00CD'   0F                      db      0f      ;    Reserved
00CE'   0F                      db      0f      ;    Reserved
00CF'   0F                      db      0f      ;    Reserved
00D0'   0F                      db      0f      ;    Reserved
00D1'   0F                      db      0f      ;    Reserved
00D2'   0F                      db      0f      ;    Reserved
00D3'   0F                      db      0f      ;    Reserved
00D4'   0F                      db      0f      ;    Reserved
00D5'   0F                      db      0f      ;    Reserved
00D6'   0F                      db      0f      ;    Reserved
00D7'   0F                      db      0f      ;    Reserved
00D8'   0F                      db      0f      ;Video  68a21  port
00D9'   0F                      db      0f      ;Video  68a21  port
00DA'   0F                      db      0f      ;Video  68a21  port
```

```
IODEC I/O decoder for the Z-100

  00DB'   0F                        db      0f      ;Video  68a21  port
  00DC'   0F                        db      0f      ;Video  68a45  CRTC
  00DD'   0F                        db      0f      ;Video  68a45  CRTC
  00DE'   0F                        db      0f      ;Video light pen counter
  00DF'   0F                        db      0f      ;    Reserved
                                    page
```

SEMICONDUCTOR IDENTIFICATION

```
IODEC I/O decoder for the Z-100


00E0'   0B                      db      0b      ;68a21 Printer port
00E1'   0B                      db      0b      ;68a21 Printer port
00E2'   0B                      db      0b      ;68a21 Printer port
00E3'   0B                      db      0b      ;68a21 Printer port
00E4'   0B                      db      0b      ;8253  Timer   port
00E5'   0B                      db      0b      ;8253  Timer   port
00E6'   0B                      db      0b      ;8253  Timer   port
00E7'   0B                      db      0b      ;8253  Timer   port
00E8'   03                      db      03      ;Serial A   Printer     DIO bus
00E9'   03                      db      03      ;Serial A   Printer     DIO bus
00EA'   03                      db      03      ;Serial A   Printer     DIO bus
00EB'   03                      db      03      ;Serial A   Printer     DIO bus
00EC'   03                      db      03      ;Serial B     Modem     DIO bus
00ED'   03                      db      03      ;Serial B     Modem     DIO bus
00EE'   03                      db      03      ;Serial B     Modem     DIO bus
00EF'   03                      db      03      ;Serial B     Modem     DIO bus
00F0'   0D                      db      0d      ;8259a  Slave  port
00F1'   0D                      db      0d      ;8259a  Slave  port
00F2'   0D                      db      0d      ;8259a Master  port
00F3'   0D                      db      0d      ;8259a Master  port
00F4'   05                      db      05      ;8041a     Keyboard     DIO bus
00F5'   05                      db      05      ;8041a     Keyboard     DIO bus
00F6'   0F                      db      0f      ;    Reserved
00F7'   0F                      db      0f      ;    Reserved
00F8'   0F                      db      0f      ;    Reserved
00F9'   0F                      db      0f      ;    Reserved
00FA'   0F                      db      0f      ;    Reserved
00FB'   0E                      db      0e      ;8253  Timer Status
00FC'   0E                      db      0e      ;Memory control
00FD'   0E                      db      0e      ;High-Address latch
00FE'   0E                      db      0e      ;CPU   Swap    port
00FF'   06                      db      06      ;Dip Switch    port     DIO bus

                                end
```

```
IODEC I/O decoder for the Z-100

Macros:

Symbols:


No  Fatal error(s)
```

SEMICONDUCTOR IDENTIFICATION

```
                        ;       MEMDEC - MEMORY MAPPING ROM
                        ;
                        ;       ZDS part no.:   444-104
                        ;       release date:   5/25/82
                        ;              prom:    82s129(256x4)
                        ;          checksum:    0740
                        ;
                        ;
                                ORG 00H
                        ;
                        ;
                        ;       ADDRESS INPUTS ARE AS FOLLOWS:
                        ;
                        ;       A7 ---- MAPSEL1
                        ;       A6 ---- MAPSEL0
                        ;       A5 ---- BA17
                        ;       A4 ---- BA16
                        ;       A3 ---- BA15
                        ;       A2 ---- BA14
                        ;       A1 ---- BA13
                        ;       A0 ---- BA12
                        ;
                        ;
                        ;       PROM OUTPUTS ARE AS FOLLOWS:
                        ;
                        ;       O3 ----  BSEL    (PIN 9, MSB)
                        ;       O2 ----  REN2
                        ;       O1 ----  REN1
                        ;       O0 ----  REN0    (PIN 12, LSB)
                        ;
                        ;*************************************************************
                        ;       MAP 0
                        ;*************************************************************
                        ;
0000'   06                      DB      06H
0001'   06                      DB      06H
0002'   06                      DB      06H
0003'   06                      DB      06H
0004'   06                      DB      06H
0005'   06                      DB      06H
0006'   06                      DB      06H
0007'   06                      DB      06H
0008'   06                      DB      06H
0009'   06                      DB      06H
000A'   06                      DB      06H
000B'   06                      DB      06H
```

SEMICONDUCTOR IDENTIFICATION

```
000C'   06                      DB      06H
000D'   06                      DB      06H
000E'   06                      DB      06H
000F'   06                      DB      06H
                        ;
0010'   05                      DB      05H
0011'   05                      DB      05H
0012'   05                      DB      05H
0013'   05                      DB      05H
0014'   05                      DB      05H
0015'   05                      DB      05H
0016'   05                      DB      05H
0017'   05                      DB      05H
0018'   05                      DB      05H
0019'   05                      DB      05H
001A'   05                      DB      05H
001B'   05                      DB      05H
001C'   05                      DB      05H
001D'   05                      DB      05H
001E'   05                      DB      05H
001F'   05                      DB      05H
                        ;
0020'   03                      DB      03H
0021'   03                      DB      03H
0022'   03                      DB      03H
0023'   03                      DB      03H
0024'   03                      DB      03H
0025'   03                      DB      03H
0026'   03                      DB      03H
0027'   03                      DB      03H
0028'   03                      DB      03H
0029'   03                      DB      03H
002A'   03                      DB      03H
002B'   03                      DB      03H
002C'   03                      DB      03H
002D'   03                      DB      03H
002E'   03                      DB      03H
002F'   03                      DB      03H
                        ;
0030'   0F                      DB      0FH
0031'   0F                      DB      0FH
0032'   0F                      DB      0FH
0033'   0F                      DB      0FH
0034'   0F                      DB      0FH
0035'   0F                      DB      0FH
0036'   0F                      DB      0FH
```

SEMICONDUCTOR IDENTIFICATION

```
0037'  0F                       DB      0FH
0038'  0F                       DB      0FH
0039'  0F                       DB      0FH
003A'  0F                       DB      0FH
003B'  0F                       DB      0FH
003C'  0F                       DB      0FH
003D'  0F                       DB      0FH
003E'  0F                       DB      0FH
003F'  0F                       DB      0FH
                        ;
                        ;*************************************************************
                        ;       MAP 1
                        ;*************************************************************
                        ;
                        ;
0040'  05                       DB      05H
0041'  05                       DB      05H
0042'  05                       DB      05H
0043'  05                       DB      05H
0044'  05                       DB      05H
0045'  05                       DB      05H
0046'  05                       DB      05H
0047'  05                       DB      05H
0048'  05                       DB      05H
0049'  05                       DB      05H
004A'  05                       DB      05H
004B'  05                       DB      05H
004C'  06                       DB      06H
004D'  06                       DB      06H
004E'  06                       DB      06H
004F'  06                       DB      06H
                        ;
0050'  06                       DB      06H
0051'  06                       DB      06H
0052'  06                       DB      06H
0053'  06                       DB      06H
0054'  06                       DB      06H
0055'  06                       DB      06H
0056'  06                       DB      06H
0057'  06                       DB      06H
0058'  06                       DB      06H
0059'  06                       DB      06H
005A'  06                       DB      06H
005B'  06                       DB      06H
005C'  05                       DB      05H
005D'  05                       DB      05H
```

```
005E'   05                      DB      05H
005F'   05                      DB      05H
                        ;
0060'   03                      DB      03H
0061'   03                      DB      03H
0062'   03                      DB      03H
0063'   03                      DB      03H
0064'   03                      DB      03H
0065'   03                      DB      03H
0066'   03                      DB      03H
0067'   03                      DB      03H
0068'   03                      DB      03H
0069'   03                      DB      03H
006A'   03                      DB      03H
006B'   03                      DB      03H
006C'   03                      DB      03H
006D'   03                      DB      03H
006E'   03                      DB      03H
006F'   03                      DB      03H
                        ;
0070'   0F                      DB      0FH
0071'   0F                      DB      0FH
0072'   0F                      DB      0FH
0073'   0F                      DB      0FH
0074'   0F                      DB      0FH
0075'   0F                      DB      0FH
0076'   0F                      DB      0FH
0077'   0F                      DB      0FH
0078'   0F                      DB      0FH
0079'   0F                      DB      0FH
007A'   0F                      DB      0FH
007B'   0F                      DB      0FH
007C'   0F                      DB      0FH
007D'   0F                      DB      0FH
007E'   0F                      DB      0FH
007F'   0F                      DB      0FH
                        ;
                        ;*******************************************************
                        ;       MAP 2
                        ;*******************************************************
                        ;
                        ;
0080'   03                      DB      03H
0081'   03                      DB      03H
0082'   03                      DB      03H
0083'   03                      DB      03H
```

SEMICONDUCTOR IDENTIFICATION

```
0084'  03                    DB      03H
0085'  03                    DB      03H
0086'  03                    DB      03H
0087'  03                    DB      03H
0088'  03                    DB      03H
0089'  03                    DB      03H
008A'  03                    DB      03H
008B'  03                    DB      03H
008C'  06                    DB      06H
008D'  06                    DB      06H
008E'  06                    DB      06H
008F'  06                    DB      06H
                        ;
0090'  05                    DB      05H
0091'  05                    DB      05H
0092'  05                    DB      05H
0093'  05                    DB      05H
0094'  05                    DB      05H
0095'  05                    DB      05H
0096'  05                    DB      05H
0097'  05                    DB      05H
0098'  05                    DB      05H
0099'  05                    DB      05H
009A'  05                    DB      05H
009B'  05                    DB      05H
009C'  05                    DB      05H
009D'  05                    DB      05H
009E'  05                    DB      05H
009F'  05                    DB      05H
                        ;
00A0'  06                    DB      06H
00A1'  06                    DB      06H
00A2'  06                    DB      06H
00A3'  06                    DB      06H
00A4'  06                    DB      06H
00A5'  06                    DB      06H
00A6'  06                    DB      06H
00A7'  06                    DB      06H
00A8'  06                    DB      06H
00A9'  06                    DB      06H
00AA'  06                    DB      06H
00AB'  06                    DB      06H
00AC'  03                    DB      03H
00AD'  03                    DB      03H
00AE'  03                    DB      03H
00AF'  03                    DB      03H
```

```
                                ;
00B0'   0F                              DB      0FH
00B1'   0F                              DB      0FH
00B2'   0F                              DB      0FH
00B3'   0F                              DB      0FH
00B4'   0F                              DB      0FH
00B5'   0F                              DB      0FH
00B6'   0F                              DB      0FH
00B7'   0F                              DB      0FH
00B8'   0F                              DB      0FH
00B9'   0F                              DB      0FH
00BA'   0F                              DB      0FH
00BB'   0F                              DB      0FH
00BC'   0F                              DB      0FH
00BD'   0F                              DB      0FH
00BE'   0F                              DB      0FH
00BF'   0F                              DB      0FH
                                ;
                                ;
                                ;*****************************************************************
                                ;       MAP 3
                                ;*****************************************************************
                                ;
                                ;
00C0'   06                              DB      06H
00C1'   05                              DB      05H
00C2'   05                              DB      05H
00C3'   05                              DB      05H
00C4'   05                              DB      05H
00C5'   05                              DB      05H
00C6'   05                              DB      05H
00C7'   05                              DB      05H
00C8'   05                              DB      05H
00C9'   05                              DB      05H
00CA'   05                              DB      05H
00CB'   05                              DB      05H
00CC'   05                              DB      05H
00CD'   05                              DB      05H
00CE'   05                              DB      05H
00CF'   06                              DB      06H
                                ;
00D0'   05                              DB      05H
00D1'   06                              DB      06H
00D2'   06                              DB      06H
00D3'   06                              DB      06H
00D4'   06                              DB      06H
```

SEMICONDUCTOR IDENTIFICATION

```
00D5'   06                      DB      06H
00D6'   06                      DB      06H
00D7'   06                      DB      06H
00D8'   06                      DB      06H
00D9'   06                      DB      06H
00DA'   06                      DB      06H
00DB'   06                      DB      06H
00DC'   06                      DB      06H
6pDD'!  06                      DB      06H
00DE'   06                      DB      06H
00DF'   05                      DB      05H
                        ;
00E0'   03                      DB      03H
00E1'   03                      DB      03H
00E2'   03                      DB      03H
00E3'   03                      DB      03H
00E4'   03                      DB      03H
00E5'   03                      DB      03H
00E6'   03                      DB      03H
00E7'   03                      DB      03H
00E8'   03                      DB      03H
00E9'   03                      DB      03H
00EA'   03                      DB      03H
00EB'   03                      DB      03H
00EC'   03                      DB      03H
00ED'   03                      DB      03H
00EE'   03                      DB      03H
00EF'   03                      DB      03H
                        ;
00F0'   0F                      DB      0FH
00F1'   0F                      DB      0FH
00F2'   0F                      DB      0FH
00F3'   0F                      DB      0FH
00F4'   0F                      DB      0FH
00F5'   0F                      DB      0FH
00F6'   0F                      DB      0FH
00F7'   0F                      DB      0FH
00F8'   0F                      DB      0FH
00F9'   0F                      DB      0FH
00FA'   0F                      DB      0FH
00FB'   0F                      DB      0FH
00FC'   0F                      DB      0FH
00FD'   0F                      DB      0FH
00FE'   0F                      DB      0FH
00FF'   0F                      DB      0FH
                        ;
```

SEMICONDUCTOR IDENTIFICATION

END

SEMICONDUCTOR IDENTIFICATION

```
                                title   CPU Status Decode Rom for the Z-100     ver.2

                        ;       ZDS part no.:   444-105
                        ;       release date:   5/25/82
                        ;               prom:   82s123(32x8)
                        ;           checksum:   0538

0000'                           aseg
                                org     0
                        ;                       __D7 = WAIT
                        ;                      /__D6 = sM1
                        ;                     //__D5 = sOUT
                        ;                    ///__D4 = sINP
                        ;                   ////__D3 = sMEMR
                        ;                  /////__D2 = sHLTA
                        ;                 //////__D1 = sINTA
                        ;                ///////__D0 = sWO
                        ;                ////////
0000    05              _0:     db      00000101b       ;05h    85 sHLTA
0001    09                      db      00001001b       ;09h    85 sMEMR
0002    00                      db      00000000b       ;00h    85 sWO*
0003    49                      db      01001001b       ;49h    85 sM1
0004    05                      db      00000101b       ;05h    85 sHLTA
0005    91              _5:     db      10010001b       ;91h    85 sINP
0006    A0                      db      10100000b       ;a0h    85 sOUT
0007    83                      db      10000011b       ;83h    85 sINTA
0008    49                      db      01001001b       ;49h    88 sM1
0009    09                      db      00001001b       ;09h    88 sMEMR
000A    00              _10:    db      00000000b       ;00h    88 sWO*
000B    01                      db      00000001b       ;01h    not defined
000C    83                      db      10000011b       ;83h    88 sINTA
000D    91                      db      10010001b       ;91h    88 sINP
000E    A0                      db      10100000b       ;a0h    88 sOUT
000F    05              _15:    db      00000101b       ;05h    88 sHLTA
0010    05                      db      00000101b       ;05h    85 sHLTA
0011    09                      db      00001001b       ;09h    85 sMEMR
0012    00                      db      00000000b       ;00h    85 sWO*
0013    49                      db      01001001b       ;49h    85 sM1
0014    05              _20:    db      00000101b       ;05h    85 sHLTA
0015    11                      db      00010001b       ;11h    85 sINP
0016    20                      db      00100000b       ;20h    85 sOUT
0017    03                      db      00000011b       ;03h    85 sINTA
0018    49                      db      01001001b       ;49h    88 sM1
0019    09              _25:    db      00001001b       ;09h    88 sMEMR
001A    00                      db      00000000b       ;00h    88 sWO*
001B    01                      db      00000001b       ;01h    not defined
```

SEMICONDUCTOR IDENTIFICATION

```
CPU Status Decode Rom for the Z-100      ver.2

  001C    03                        db      00000011b       ;03h    88 sINTA
  001D    11                        db      00010001b       ;11h    88 sINP
  001E    20              _30:      db      00100000b       ;20h    88 sOUT
  001F    05                        db      00000101b       ;05h    88 sHLTA
                                    end
```

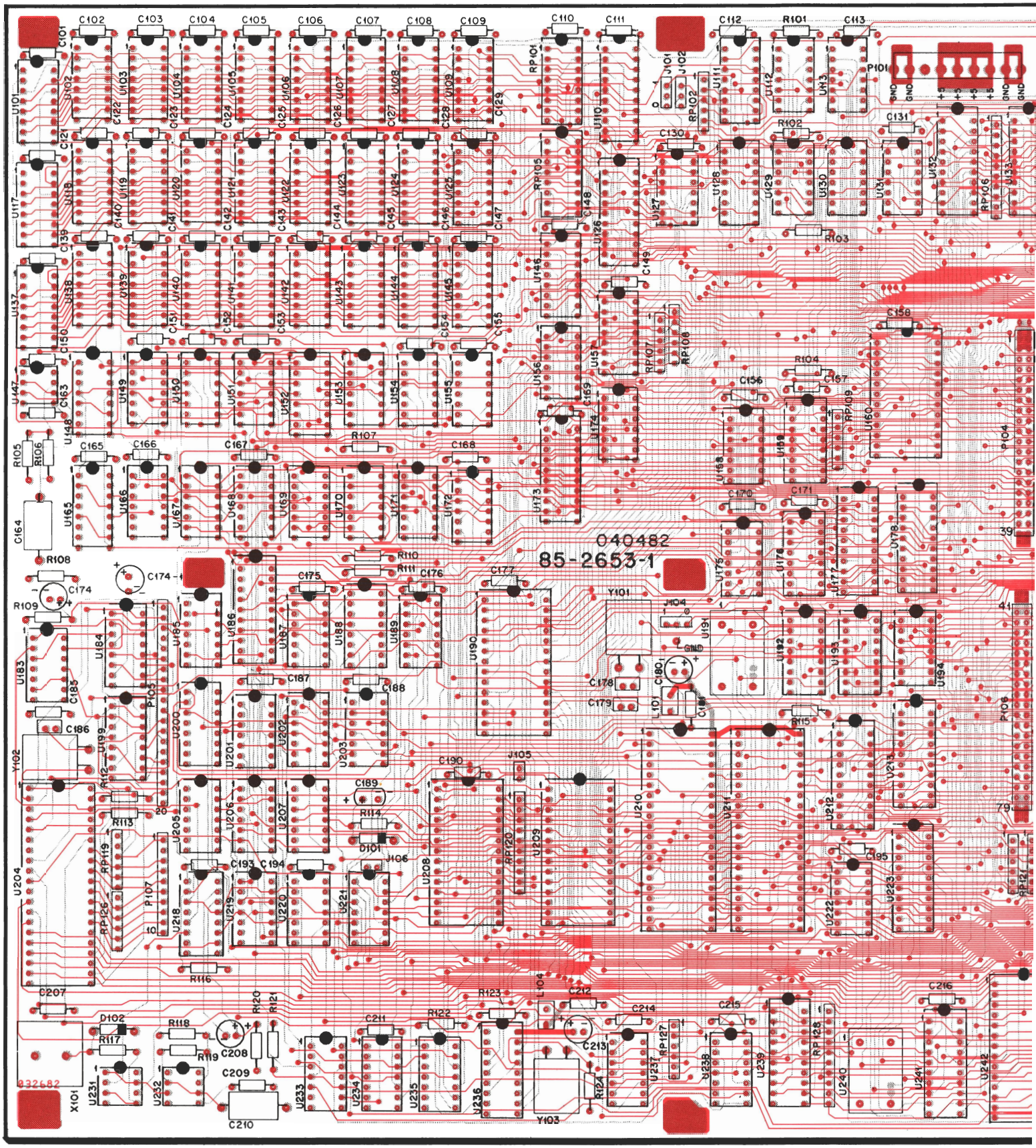
CIRCUIT BOARD X-RAY VIEW

NOTE: To find the PART NUMBER of a component for the purpose of ordering a replacement part:

A. Find the circuit component number (R5, C3, etc.) on the X-Ray View.

B. Locate this same number in the "Circuit Component Number" column of the "Parts List."

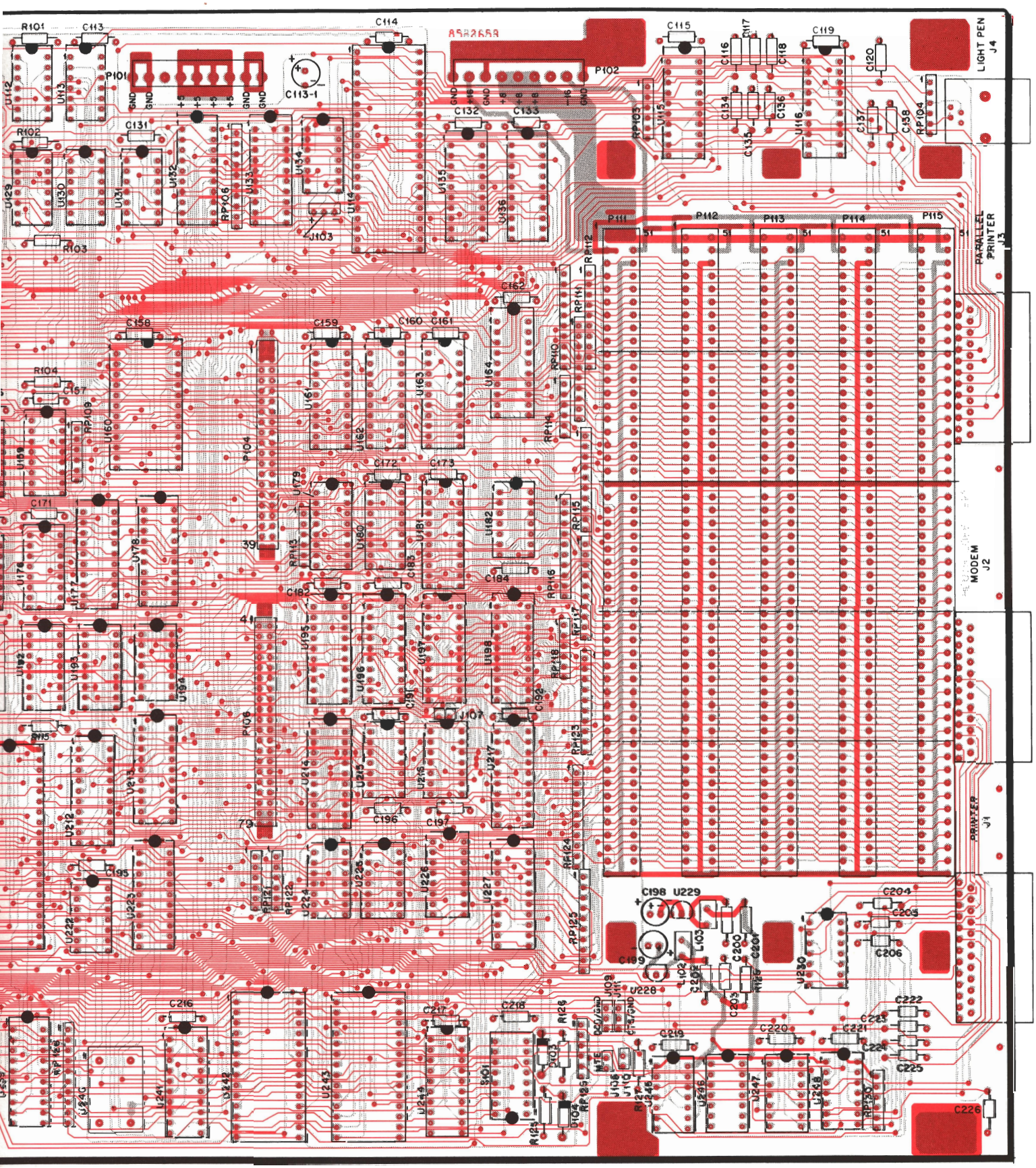
C. Adjacent to the circuit component number, you will find the PART NUMBER and DESCRIPTION which must be supplied when you order a replacement part.



MAIN CIRCUIT BOARD

Component side shown in r

foil side shown in gray.



MAIN CIRCUIT BOARD

Component side shown in red, foil side shown in gray.

INTERCONNECT PIN DEFINITIONS

S-100 Bus Definitions

The definitions of the S-100 bus pins are given in the Appendix A portion of this documentation.

RS-232 Pin Definitions

The following chart gives the definitions of the RS-232 Serial Port pins.

RS-232C Interface Signals

Pin	Description
1	Protective ground
2	Transmitted data
3	Received data
4	Request to send
5	Clear to send
6	Data set ready
7	Signal ground (common return)
8	Received line signal detector
9	(Reserved for data set testing)
10	(Reserved for data set testing)
11	Unassigned
12	Secondary received line signal detector
13	Secondary clear to send
14	Secondary transmitted data
15	Transmission signal element timing (DCE source)
16	Secondary received data
17	Receiver signal element timing (DCE source)
18	Unassigned
19	Secondary request to send
20	Data terminal ready
21	Signal quality detector
22	Ring indicator
23	Data signal rate selector (DTE/DCE source)
24	Transmit signal element timing (DTE source)
25	Unassigned

INTERCONNECT PIN DEFINITIONS

Parallel Port Definitions

The chart below gives the definition of the parallel port.

Parallel Port Pinout

PIN	SIGNAL NAME	FUNCTION
1	STROBE	A pulse that clocks data.
2	PDATA1	Data to the peripheral.
3	PDATA2	Data to the peripheral.
4	PDATA3	Data to the peripheral.
5	PDATA4	Data to the peripheral.
6	PDATA5	Data to the peripheral.
7	PDATA6	Data to the peripheral.
8	PDATA7	Data to the peripheral.
9	PDATA8	Data to the peripheral.
10	ACKNLG	Acknowledge signal from the printer.
11	BUSY	Printer not ready for data when this signal is high.
12	GND	Ground.
15	ERROR	Error signal from the printer when this signal is low.
16	INIT	Pulse signal that initializes the printer.
17	GND	Ground.
18	GND	Ground.
19	GND	Ground.
20	GND	Ground.
21	GND	Ground.
22	GND	Ground.
23	GND	Ground.
24	GND	Ground.
25	GND	Ground.

INTERCONNECT PIN DEFINITIONS

Light Pen Definitions

The following chart gives the definition of the light pen port.

PIN	SIGNAL NAME	FUNCTION
1	+5V	Plus 5-volt supply
2	LTPNSW	Monitors light pen switch
3	LTPEN	Light pen "hit" signal
4	GND	Ground

Keyboard Connector Definitions

The following chart gives the definitions of the keyboard cable connectors.

Connector P105

PIN	SIGNAL NAME	FUNCTION
1	COL15	Column 15 line
2	CTRL	CONTROL line
3	COL8	Column 8 line
4	KBRST	Keyboard reset line
5	COL12	Column 12 line
6	COL14	Column 14 line
7	COL9	Column 9 line
8	COL13	Column 13 line
9	COL4	Column 4 line
10	COL10	Column 10 line
11	COL1	Column 1 line
12	COL5	Column 5 line
13	COL3	Column 3 line
14	COL11	Column 11 line
15	COL0	Column 0 line
16	COL2	Column 2 line
17	COL6	Column 6 line
18	COL7	Column 7 line
19	LED ANODE	LED anode line
20	LED CATHODE	LED cathode line

INTERCONNECT PIN DEFINITIONS

Connector P107

PIN	SIGNAL NAME	FUNCTION
1	SHIFT ROW	Shift row line
2	CTRL/RESET	Control (CTRL) and RESET line
3	ROW0	Row 0 line
4	ROW1	Row 1 line
5	ROW2	Row 2 line
6	ROW3	Row 3 line
7	ROW4	Row 4 line
8	ROW5	Row 5 line
9	ROW6	Row 6 line
10	ROW7	Row 7 line

INTERCONNECT PIN DEFINITIONS

Video Logic Board Connectors

The following charts give the definitions of the video logic circuit board connectors.

Connector P104

PIN	SIGNAL NAME	FUNCTION
1	+5VDC	+ 5-volt supply line
2	+5VDC	+ 5-volt supply line
3	+5VDC	+ 5-volt supply line
4	+5VDC	+ 5-volt supply line
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	BA0	
10	BA1	
11	BA1	
12	BA3	
13	BA4	
14	BA5	
15	BA6	
16	BA7	
17	BA8	
18	BA9	
19	BA10	
20	BA11	Buffered
21	BA12	Address Lines
22	BA13	
23	BA14	
24	BA15	
25	BA16	
26	BA17	
27	BA18	
28	BA19	
29	BA20	
30	BA21	
31	BA22	
32	BA23	

INTERCONNECT PIN DEFINITIONS

33	GND	Ground
34	GND	Ground
35	BD00	Data output lines
36	BD01	
37	BD02	
38	BD03	
39	GND	Ground
40	GND	Ground
41	GND	Ground
42	GND	Ground
43	BD04	Data output lines
44	BD05	
45	BD06	
46	BD07	
47	GND	Ground
48	GND	Ground
49	BDI0	Data input lines
50	BDI1	
51	BDI2	
52	BDI3	
53	BDI4	
54	BDI5	
55	BDI6	
56	BDI7	
57	$\overline{\text{RDBFRENBL}}$	Read buffer enable
58	NC	No connection
59	GND	Ground
60	GND	Ground
61	$\overline{\text{CRTRAMSEL}}$	CRT RAM select
62	VIDRAMRDY	Video RAM ready
63	LTPNSTB	Light pen strobe
64	POC*	Power-on clear
65	$\overline{\text{RESET2}}$	Reset
66	ECLK	E clock
67	OUT	Output status signal
68	$\overline{\text{OUT}}$	
69	MEMR	Status memory read

INTERCONNECT PIN DEFINITIONS

70	STVAL*SYNC	Status valid signal
71	BMWRT	Buffered memory write
72	$\overline{WO}$	Status write
73	$\overline{WR}$	Write strobe
74	$\overline{IO}$	Chip-select line
75	$\overline{DBIN}$	Data request control signal
76	VIDINT	Video Interrupt
77	GND	Ground
78	GND	Ground
79	GND	Ground
80	GND	Ground

INTERCONNECT PIN DEFINITIONS

Power Supply Connectors

The following charts give the definitions of the power supply connectors.

PIN	SIGNAL NAME	FUNCTION
1	GND	Ground
2	GND	Ground
3		No connection
4	+5	Plus 5-volt supply
5	+5	Plus 5-volt supply
6	+5	Plus 5-volt supply
7	+5	Plus 5-volt supply
8	GND	Ground
9	GND	Ground

Connector P102

PIN	SIGNAL NAME	FUNCTION
1	GND	Ground
2	+16	Plus 16-volt supply
3	GND	Ground
4	+8	Plus 8-volt supply
5	+8	Plus 8-volt supply
6	+8	Plus 8-volt supply
7		No connection
8	−16	Minus 16-volt supply
9	GND	Ground

Keyboard Encoder

DESCRIPTION

The keyboard encoder (or processor) scans the keyboard matrix to determine if a key has been pushed down. After finding a "down" key, it then sends a corresponding key code to the system to indicate which key is down. This is its normal ASCII mode of operation.

When in its event-driven mode (an alternate "up/down" mode), it not only sends a "down code," but it also sends a different "up code" when the key is released. In this mode, the codes transmitted are arbitrary and do not directly relate to the key's ASCII character. However, the codes are unique for each key.

Other functions that the keyboard encoder provides are:

- Autorepeat on/off — 11 keys per second, when selected
- Fast repeat rate — 28 keys per second
- Key debounce — 5 milliseconds maximum
- Key click on/off
- Clear FIFO (First In First Out) buffer
- Beep sound (software produced, not produced by key closure)
- Keyboard enable/disable

The scanning method is as follows. The encoder sends a key code to the master processor when it finds a key that is down. It then continues to scan until it finds another key down, and outputs its code to the master processor also. Then the encoder stops scanning and interrogates these two keys until one of them is released; in which case, scanning resumes. This applies only to the ASCII mode of operation. In the event-driven mode, the encoder never stops scanning.

Power Configuration

After power-up or a hard reset, the keyboard encoder is initialized to the following state:

- Autorepeat is enabled.
- Key click is enabled.
- The FIFO and the output buffer are cleared.
- The keyboard encoder is in the ASCII scan mode.

Software Controllable Features

The following features are software controllable.

AUTOREPEAT — A key is repeated when it is held down. This option may be disabled by software. Also, it can not be selected when in the event-driven (up/down) mode.

KEY CLICK — A click sound is produced when a key is pressed. This function may also be disabled and enabled by software. When in the event-driven mode, a click is produced when a key is pressed and another click is produced when the key is released.

FIFO — The keyboard encoder maintains a 17-key FIFO (first in, first out) buffer in case the master processor cannot service the keyboard immediately. 17 keystrokes can be stored until the master processor is free to service the keyboard. Once the FIFO is full, any keys pressed will be lost because keyboard scanning stops until there is room in the FIFO. The FIFO may be cleared by software, but the data register of the keyboard processor will still contain one key which may be cleared only by reading the register.

EVENT-DRIVEN (UP/DOWN) MODE — When placed in this mode, the keyboard encoder sends a unique (non-standard) code with bit 7 cleared each time a key is pressed, and sends the same code with bit 7 set when the key is released.

USER OPTIONS AND PROGRAMMING

Programming Specifications

Command port address	—	F5 (hex)
Data port address	—	F4 (hex)
Status port address	—	F5 (hex)

I/O Protocol

All I/O to the keyboard should obey the following rules.

Output To Keyboard Encoder

- Wait until $\overline{\text{KPR}}$ (Keyboard Processor Ready) is true (zero). This is found by reading the status port; port F5, bit 1 (D1).

- Output the command to the command port of the keyboard encoder.

- There is no valid information which may be written to the data port. Anything written to the data port will be ignored by the keyboard encoder. Illegal commands will also be ignored by the encoder.

Input Data From Keyboard Encoder

Key codes are the only information which may be read from the data port. There are two ways to determine when a key is waiting to be read.

- Interrupts — If interrupts were selected (see "Command Summary"), an interrupt will be generated whenever a key is placed on the data port. This interrupt is an IR6 to the master 8259A and it is up to the system or user to properly set up the 8259A's. The interrupt request is cleared when the key code is read from the data port. (The IR6 interrupt is shared with the 6845 on the video board such that a video vertical sync pulse or a light pin strobe will also cause an interrupt.)

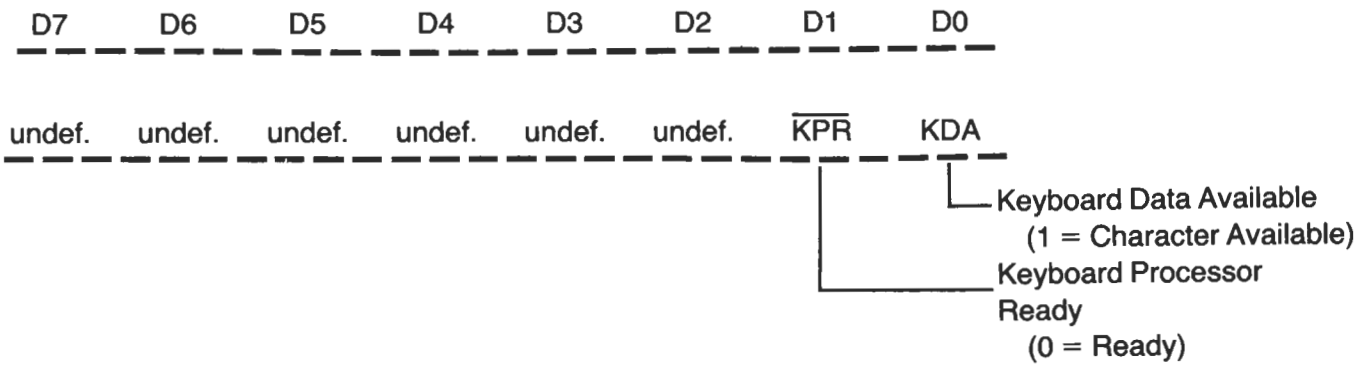
USER OPTIONS AND PROGRAMMING

- Polling — The KDA (Keyboard Data Available) bit of the status register will always be set when a key is placed on the data port. The bit is cleared when the data port is read.

Input Status From Keyboard Encoder

The status port may be read at any time without disturbing the operation of the keyboard. The bits of the status port are defined as follows:

STATUS REGISTER



KPR — Keyboard Processor Ready. This bit is set to "1" when a byte is output to the keyboard. KDA is cleared to "0" when the keyboard is ready for input.

KDA — Keyboard Data Available. Indicates that there is a key ready to be read at the data port. KPR is cleared by reading the data port.

USER OPTIONS AND PROGRAMMING

Command Summary

COMMAND	CODE (hex)
Reset	00
Autorepeat ON	01
Autorepeat OFF	02
Key click ON	03
Key click OFF	04
Clear FIFO	05
Click	06
Beep	07
Enable keyboard	08
Disable keyboard	09
Event driven mode	0A
ASCII scan mode	0B
Enable Interrupts	0C
Disable Interrupts	0D

Command Definitions

RESET — Restores the keyboard encoder to its power-up configuration with the following exception:

> The RESET command will not clear the data register of the keyboard processor. The only way to do this is by reading the data register.

AUTOREPEAT ON — Enables the autorepeat function. Autorepeat causes a key to be repeated when it is held down. This option is not available in the event-driven mode.

AUTOREPEAT OFF — Disables the autorepeat function.

KEY CLICK ON — Causes a click sound to be heard whenever a key is pressed. When in the ASCII scanning mode, the SHIFT, FAST REPEAT, CTRL, CAPS LOCK, and RESET keys do not produce clicks. When in the event-driven mode, all keys produce two clicks (one down and one up) except the RESET key.

KEY CLICK OFF — Disables the key click function.

CLEAR FIFO — Empties the keyboard processor's FIFO of any keys which may be in it. The data register of the keyboard encoder is not cleared by this command. Only an input from the data port will clear it.

CLICK — A software command (06) produces one click.

BEEP — A software command (07) produces a beep sound.

DISABLE KEYBOARD — Causes all keystrokes to be ignored except for a CTRL–RESET. The only ways to re-enable the keyboard are with the ENABLE KEYBOARD command, the RESET command, a power-up, or a CTRL-RESET.

ENABLE KEYBOARD — Enables the keyboard after it has been disabled by the DISABLE KEYBOARD command.

EVENT-DRIVEN (Up/Down) — Sending this command to the keyboard encoder causes a different scanning algorithm to be used such that a code is generated when a key is depressed and another code is generated when the same key is released.

Each key has a unique code including CTRL, FAST REPEAT, CAPS LOCK, and SHIFT keys. Therefore, there is no such thing as a shifted key when in this mode. Instead, a byte is output for the SHIFT key and a byte is output for the primary key.

The high order bit is used to distinguish between a key pressed and a key released. When a key is pressed, bit 7 will be 0. When a key is released, bit 7 will be 1. The RESET key is the only key which does not have a code since it cannot be scanned by the keyboard encoder.

DISABLE INTERRUPTS — Terminates the ENABLE INTERRUPTS function. The keyboard encoder must be polled to obtain a key code.

ENABLE INTERRUPTS — The keyboard processor sends an interrupt to the 8259A whenever a key code is in the output buffer.

THEORY OF OPERATION

The keyboard encoder circuitry basically consists of a Universal Peripehral Interface (UPI) microcomputer. (See the Partial Schematic.) It is a one-chip microcomputer that connects directly to the master processor data bus. The main features of this device are:

- 8-bit CPU
- 8-bit data bus interface registers
- 1K by 8 bit ROM memory
- 64 by 8 bit RAM memory
- Interval timer/event counter
- Two 8-bit TTL compatible I/O ports
- Resident clock oscillator

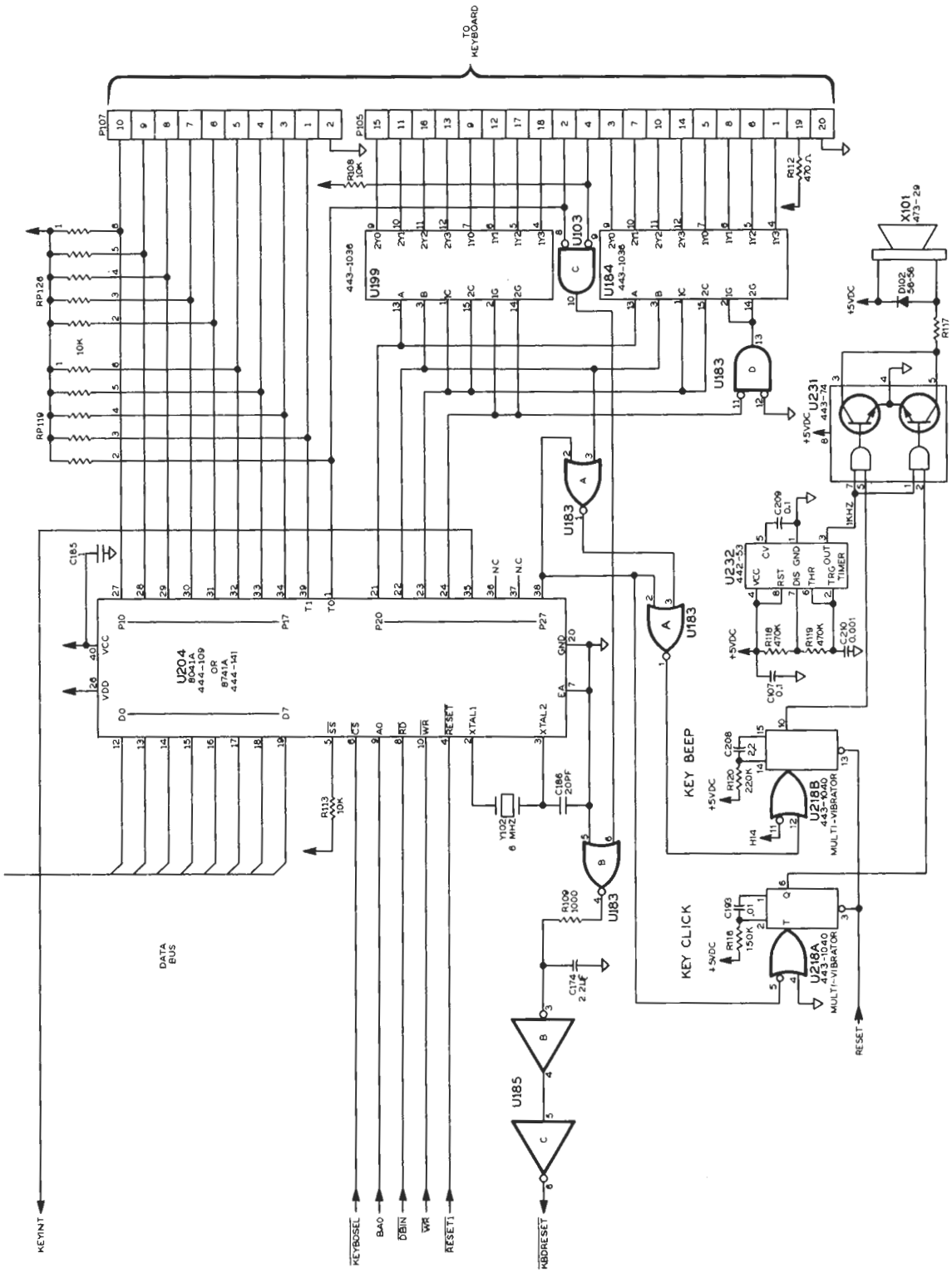
IC's U199 and U184 are dual 2-line-to-4-line decoders that function as I/O line expanders to increase the effective number of output lines from the keyboard encoder. The outputs of the line expanders are applied to the connector P105 and then to the columns of the keyboard. (See Pictorial 3-1.) When one of these output lines at P105 goes low, then any key closure (of a key attached to that particular column) will be detected as the keyboard encoder IC scans the keyboard rows (through plug P107). The encoder then puts a code on the data bus that corresponds to the detected key closure.

Pin 38 of U204 pulses to generate the bell and key clock sounds. U183 NORs this line with pin 22 to generate the bell. When U183 pin 1 goes low, it triggers the one-shot at U218B. U218 pin 10 pulses high for about 200 ms to gate U232 pin 3, the 1-kHz oscillator, through U231 to the speaker.

To generate a key click, the negative edge of pin 38 directly fires the one-shot at U218A pin 5. Pin 6 of this IC goes high for about 10 ms to gate U232 through U231 to the speaker. Note that the click line asserts whenever the bell does. However, since both circuits use the same oscillator, the click is not heard.

THEORY OF OPERATION

PARTIAL SCHEMATIC



TROUBLESHOOTING

Use the following chart to help you identify the source of problems. The chart lists conditions and possible causes for specific problems. If you cannot resolve the problem, refer to the warranty and service information supplied with your Computer.

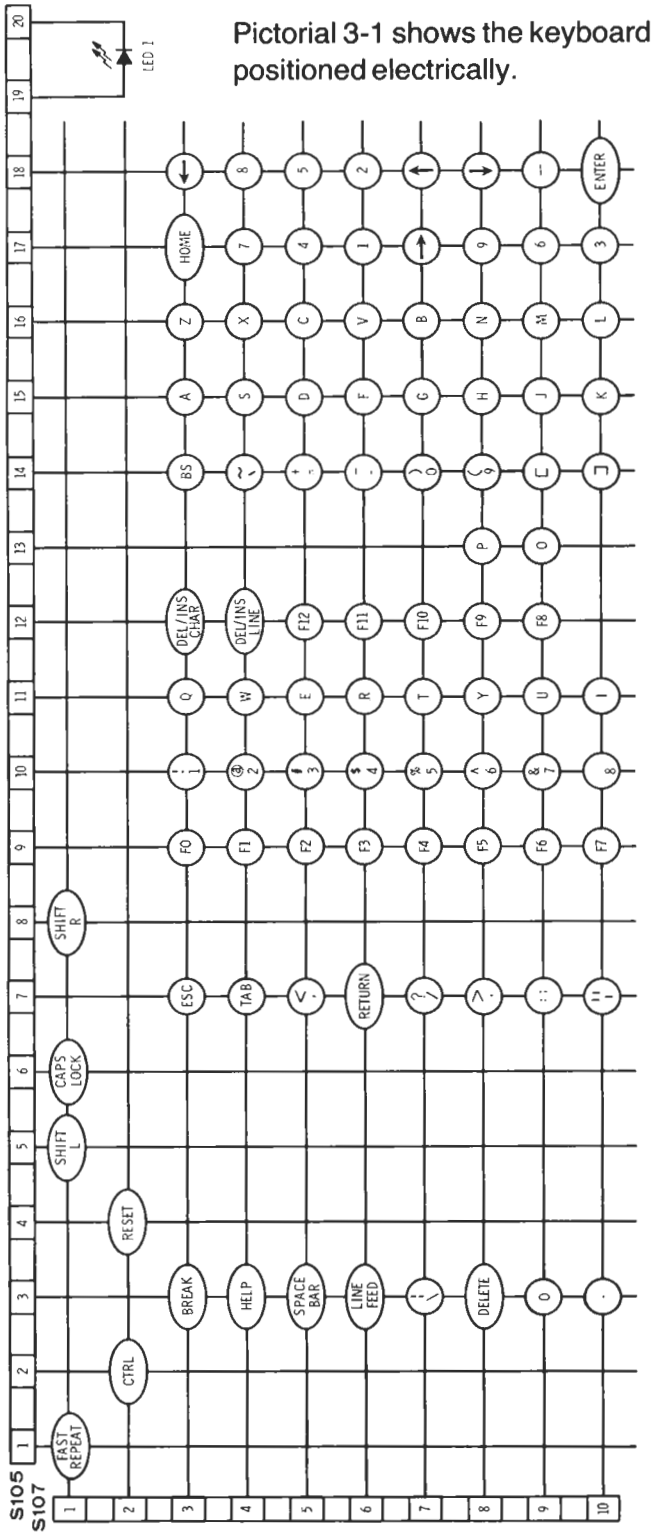
If you have electronics service skill, you may wish to service some problems yourself. In the following chart, if a particular part is mentioned, check that part and other components that are associated with it. Remember to locate and correct the cause when components are damaged, or the problem could reoccur.

Refer to the "Circuit Board X-Ray Views" for the physical location of parts on the circuit boards.

PROBLEM	POSSIBLE CAUSE
Keyboard does not function.	1. Keyboard in disabled mode. RESET the Computer. 2. Keyboard cables disconnected. 3. U204.
No key click.	1. Key click disabled. RESET the Computer.
No key click or beep.	1. Audio transducer X101. 2. U218, U231, or U232.
Autorepeat function does not work.	1. Autorepeat function is off. RESET the Computer. 2. Keyboard in event-driven mode. Select desired keyboard scan mode (ASCII mode). Autorepeat functions only in ASCII mode.
Encoder puts wrong code on data bus.	1. Keyboard in event-driven mode. Select desired keyboard scan mode (ASCII mode).
Computer will not reset.	1. RESET key always open. 2. U183 or U185, or U103. 3. CTRL key is always open.

KEYBOARD SCAN MATRIX

Pictorial 3-1 shows the keyboard scan matrix; how the keys are positioned electrically.



Pictorial 3-1
Keyboard Matrix

ENCODER OUTPUT CODES (HEX)

After a key is detected as being down, the keyboard encoder places a byte on its data bus which represents only the depressed key. The codes for some of the keys depend on the state of the "modifier" keys — SHIFT (right or left), CTRL (control), and CAPS LOCK. Some keys are not affected by any of the modifiers, such as the DELETE key. Its code (7F) is always the same, such as the DELETE key. It's code (7F) is always the same, regardless of the modifier key's positions. Other keys are affected by all of the modifiers, such as the "A" key.

In the following table, an "NC" under a modifier indicates that no code is generated for that key.

The CAPS LOCK column has a Y (yes) or N (no) to indicate if the CAPS LOCK key affects the output code or not. The CAPS LOCK key functions as a SHIFT key, but only for the alphabet keys.

Each key has a code for when it is pushed down. However, in its event-driven mode (key up/down mode), each key also has a different code for when it starts back up again. These are listed as Down Codes and Up Codes. (The "up code" equals the "down code" plus 80 hex.)

Key	Not Shifted	Shifted	Control	Control Shift	Caps Lock (Yes/No)	Down Code	Up Code
) 0	30	29	30	29	N	5B	DB
! 1	31	21	31	21	N	57	D7
@ 2	32	40	32	00	N	56	D6
# 3	33	23	33	23	N	55	D5
$ 4	34	24	34	24	N	54	D4

ENCODER OUTPUT CODES (HEX)

Key	Not Shifted	Shifted	Control	Control Shift	Caps Lock (Yes/No)	Down Code	Up Code
% 5	35	25	35	25	N	53	D3
^ 6	36	5E	36	1E	N	52	D2
& 7	37	26	37	26	N	51	D1
* 8	38	2A	38	2A	N	50	D0
(9	39	28	39	28	N	5A	DA
A	61	41	01	01	Y	07	87
B	62	42	02	02	Y	13	93
C	63	43	03	03	Y	15	95
D	64	44	04	04	Y	05	85
E	65	45	05	05	Y	0D	8D
F	66	46	06	06	Y	04	84
G	67	47	07	07	Y	03	83
H	68	48	08	08	Y	02	82
I	69	49	09	09	Y	08	88
J	6A	4A	0A	0A	Y	01	81
K	6B	4B	0B	0B	Y	00	80
L	6C	4C	0C	0C	Y	10	90

ENCODER OUTPUT CODES (HEX)

Key	Not Shifted	Shifted	Control	Control Shift	Caps Lock (Yes/No)	Down Code	Up Code
M	6D	4D	0D	0D	Y	11	91
N	6E	4E	0E	0E	Y	12	92
O	6F	4F	0F	0F	Y	19	99
P	70	50	10	10	Y	1A	9A
Q	71	51	11	11	Y	0F	8F
R	72	52	12	12	Y	0C	8C
S	73	53	13	13	Y	06	86
T	74	54	14	14	Y	0B	8B
U	75	55	15	15	Y	09	89
V	76	56	16	16	Y	14	94
W	77	57	17	17	Y	0E	8E
X	78	58	18	18	Y	16	96
Y	79	59	19	19	Y	0A	8A
Z	7A	5A	1A	1A	Y	17	97
BACK SPACE	08	08	08	08	N	5F	DF
TAB	09	09	09	09	N	4E	CE
LINE FEED	0A	0A	0A	0A	N	44	C4
RETURN	0D	0D	0D	0D	N	4C	CC

ENCODER OUTPUT CODES (HEX)

Key	Not Shifted	Shifted	Control	Control Shift	Caps Lock (Yes/No)	Down Code	Up Code
ESC	1B	1B	1B	1B	N	4F	CF
SPACE	20	20	20	20	N	45	C5
" '	27	22	27	22	N	48	C8
< ,	2C	3C	2C	3C	N	4D	CD
— -	2D	5F	2D	1F	N	5C	DC
> .	2E	3E	2E	3E	N	4A	CA
? /	2F	3F	2F	3F	N	4B	CB
: ;	3B	3A	3B	3A	N	49	C9
+ =	3D	2B	3D	2B	N	5D	DD
— [	5B	7B	1B	7B	N	59	D9
| \	5C	7C	1C	7C	N	43	C3
}]	5D	7D	1D	7D	N	58	D8
~ `	60	7E	60	7E	N	5E	DE

ENCODER OUTPUT CODES (HEX)

Key	Not Shifted	Shifted	Control	Control Shift	Caps Lock (Yes/No)	Down Code	Up Code
DELETE	7F	7F	7F	7F	N	42	C2
ENTER	8D	CD	8D	CD	N	38	B8
HELP	95	D5	95	C5	N	46	C6
F0	96	D6	96	D6	N	27	A7
F1	97	D7	97	D7	N	26	A6
F2	98	D8	98	D8	N	25	A5
F3	99	D9	99	D9	N	24	A4
F4	9A	DA	9A	DA	N	23	A3
F5	9B	DB	9B	DB	N	22	A2
F6	9C	DC	9C	DC	N	21	A1
F7	9D	DD	9D	DD	N	20	A0
F8	9E	DE	9E	DE	N	29	A9
F9	9F	DF	9F	DF	N	2A	AA
F10	A0	E0	A0	E0	N	2B	AB
F11	A1	E1	A1	E1	N	2C	AC
F12	A2	E2	A2	E2	N	2D	AD

ENCODER OUTPUT CODES (HEX)

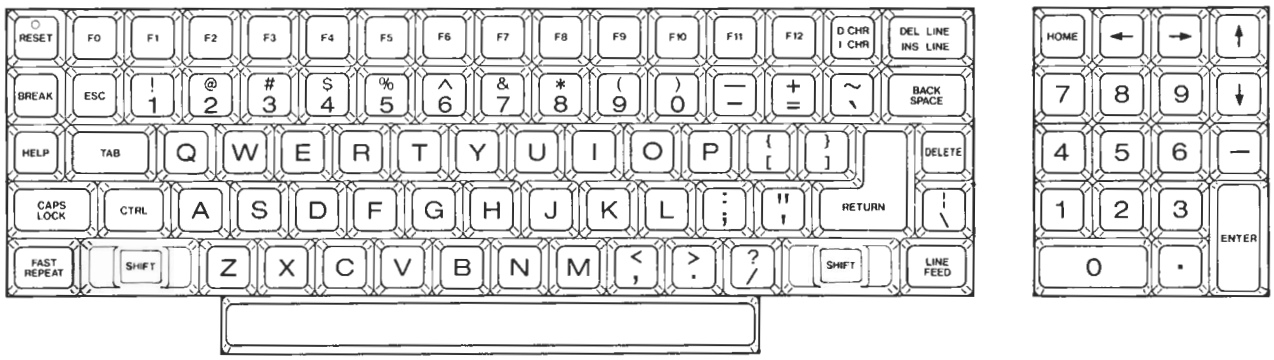
Key	Not Shifted	Shifted	Control	Control Shift	Caps Lock (Yes/No)	Down Code	Up Code
D CHR I CHR	A3	E3	A3	E3	N	2E	AE
D LINE I LINE	A4	E4	A4	E4	N	2F	AF
(up arrow)	A5	E5	A5	E5	N	3B	BB
(down arrow)	A6	E6	A6	E6	N	3A	BA
(right arrow)	A7	E7	A7	E7	N	33	B3
(left arrow)	A8	E8	A8	E8	N	3F	BF
HOME	A9	E9	A9	E9	N	37	B7
BREAK	AA	EA	AA	EA	N	47	C7
- (keypad)	AD	ED	AD	ED	N	39	B9
. (keypad)	AE	EE	AE	EE	N	40	C0
0 (keypad)	B0	F0	B0	F0	N	41	C1
1 (keypad)	B1	F1	B1	F1	N	34	B4
2 (keypad)	B2	F2	B2	F2	N	3C	BC
3 (keypad)	B3	F3	B3	F3	N	30	B0
4 (keypad)	B4	F4	B4	F4	N	35	B5
5 (keypad)	B5	F5	B5	F5	N	3D	BD
6 (keypad)	B6	F6	B6	F6	N	31	B1

ENCODER OUTPUT CODES (HEX)

Key	Not Shifted	Shifted	Control	Control Shift	Caps Lock (Yes/No)	Down Code	Up Code
7 (keypad)	B7	F7	B7	F7	N	36	B6
8 (keypad)	B8	F8	B8	F8	N	3E	BE
9 (keypad)	B9	F9	B9	F9	N	32	B2
FAST REPEAT	NC	NC	NC	NC	N	60	E0
CAPS LOCK	NC	NC	NC	NC	N	61	E1
SHIFT (right)	NC	NC	NC	NC	N	62	E2
CTRL	NC	NC	NC	NC	N	63	E3
SHIFT (left)	NC	NC	NC	NC	N	64	E4
RESET	NC	NC	(NC) Resets Computer	(NC) Resets Computer	N	NC	NC

KEYBOARD KEY LAYOUT

Pictorial 3-2 shows the key layout of the keyboard.



PICTORIAL 3-2
Keyboard Layout